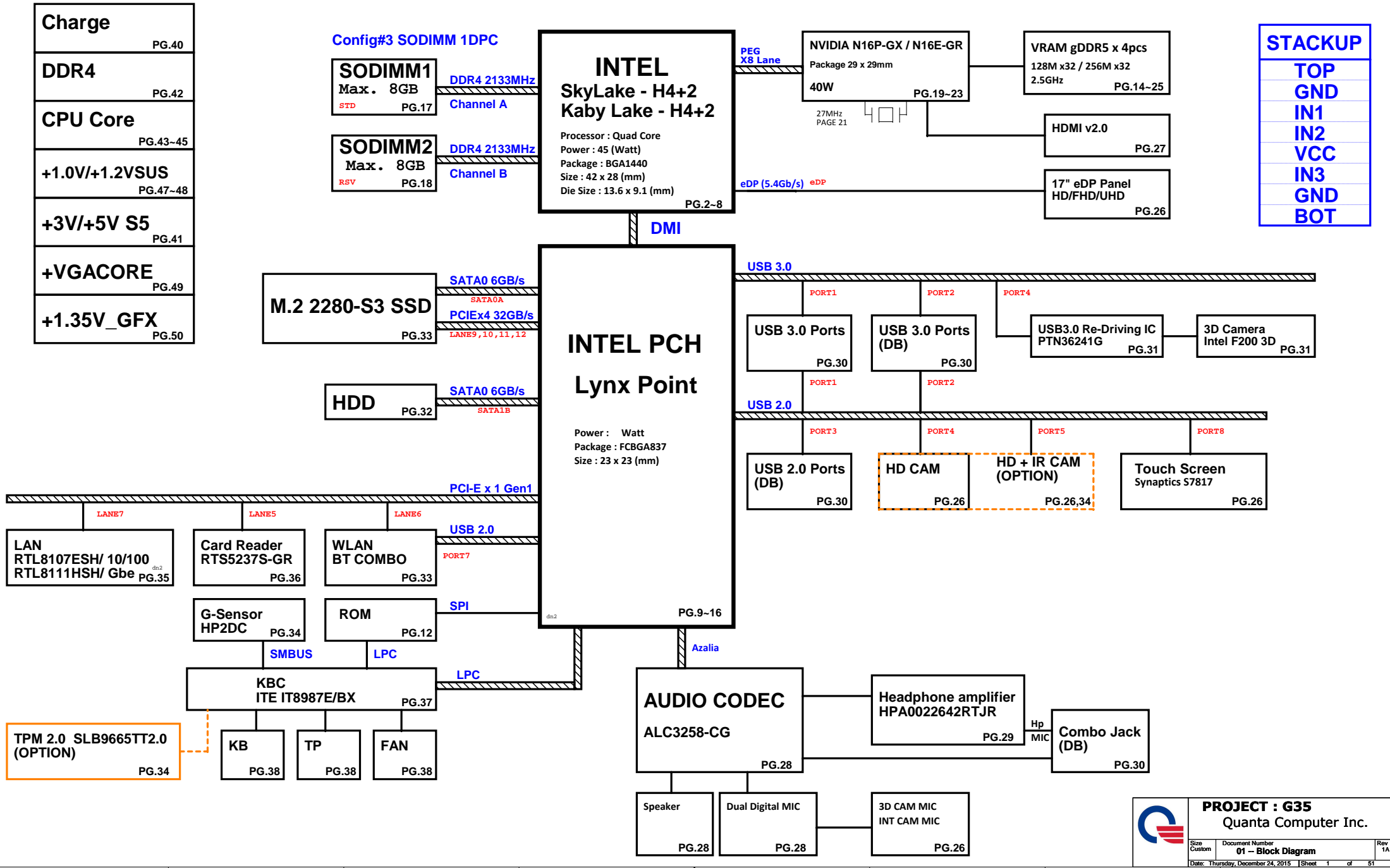
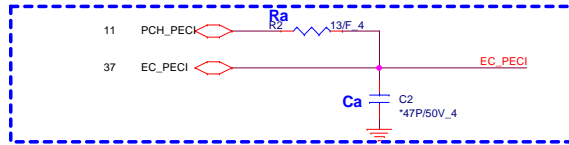


POWER PAVILION PUFF INTEL SKL / KABY -H SYSTEM DIAGRAM

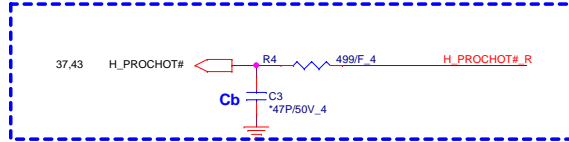
01



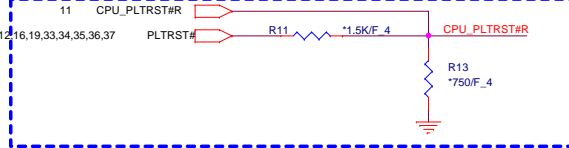
H_PECI (50ohm)
Trace Length: <0.5 inches
Ra,Ca need placement close to PCH.



PROCHOT# (50ohm)
Trace Length <11 inches
Cb need placement near VR

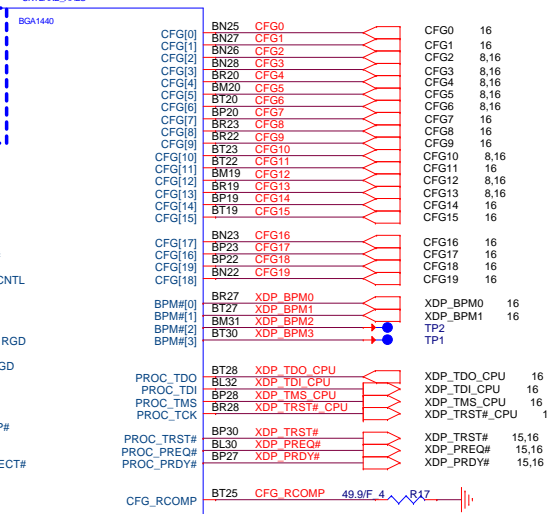
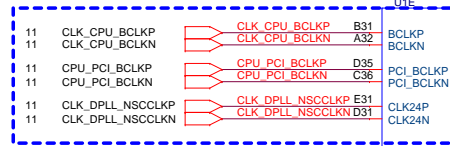


CPU_PLTRST# (50ohm)
Trace Length: 10-17 inches



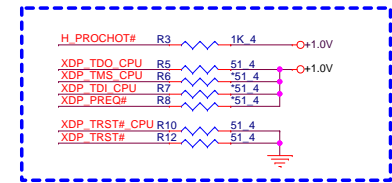
SKYLAKE Processor (CLK,MISC,JTAG)

Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impedence 90 ohm



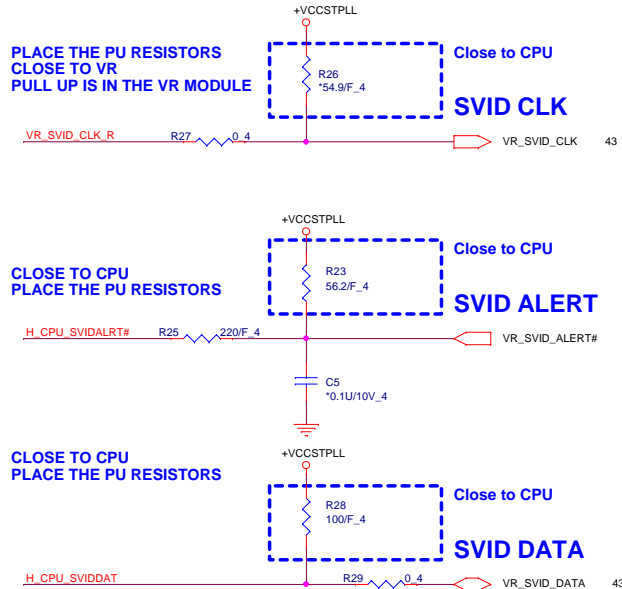
Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

Processor pull-up (CPU)

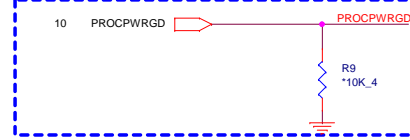


CPU CORE SVID

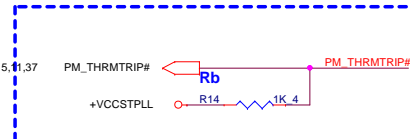
Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.



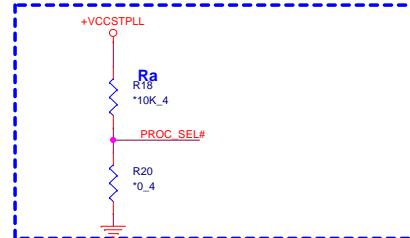
PROCPWRGD (50ohm)
Trace Length: 1-11.25 inches



THERMTRIP# (50ohm)
Trace Length: 1.1-12 inches
Rb need placement near PCH

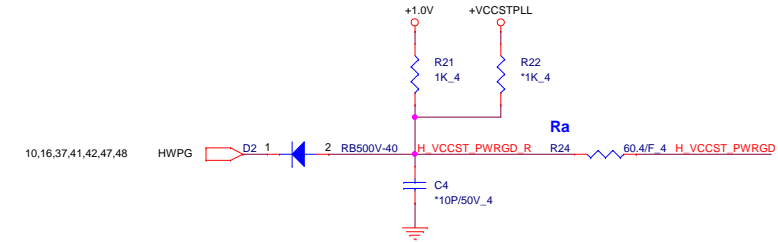


Ra(R10804) Not install in SKL-H



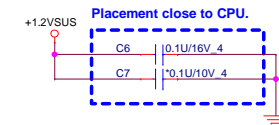
HWPD

Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A



SKYLAKE Processor (DMI,PEG,FDI)

03

dGPU

DIS : Stuff
UMA: Un-Stuff

dGPU

DMI

DMI

HDMI

eDP

11/03 modify for HDMI2.0

DP & PEG Compensation

eDP_RCOMP
Trace length < 100 Mils
Trace Width 20 Mils Trace Spacing 25 Mils

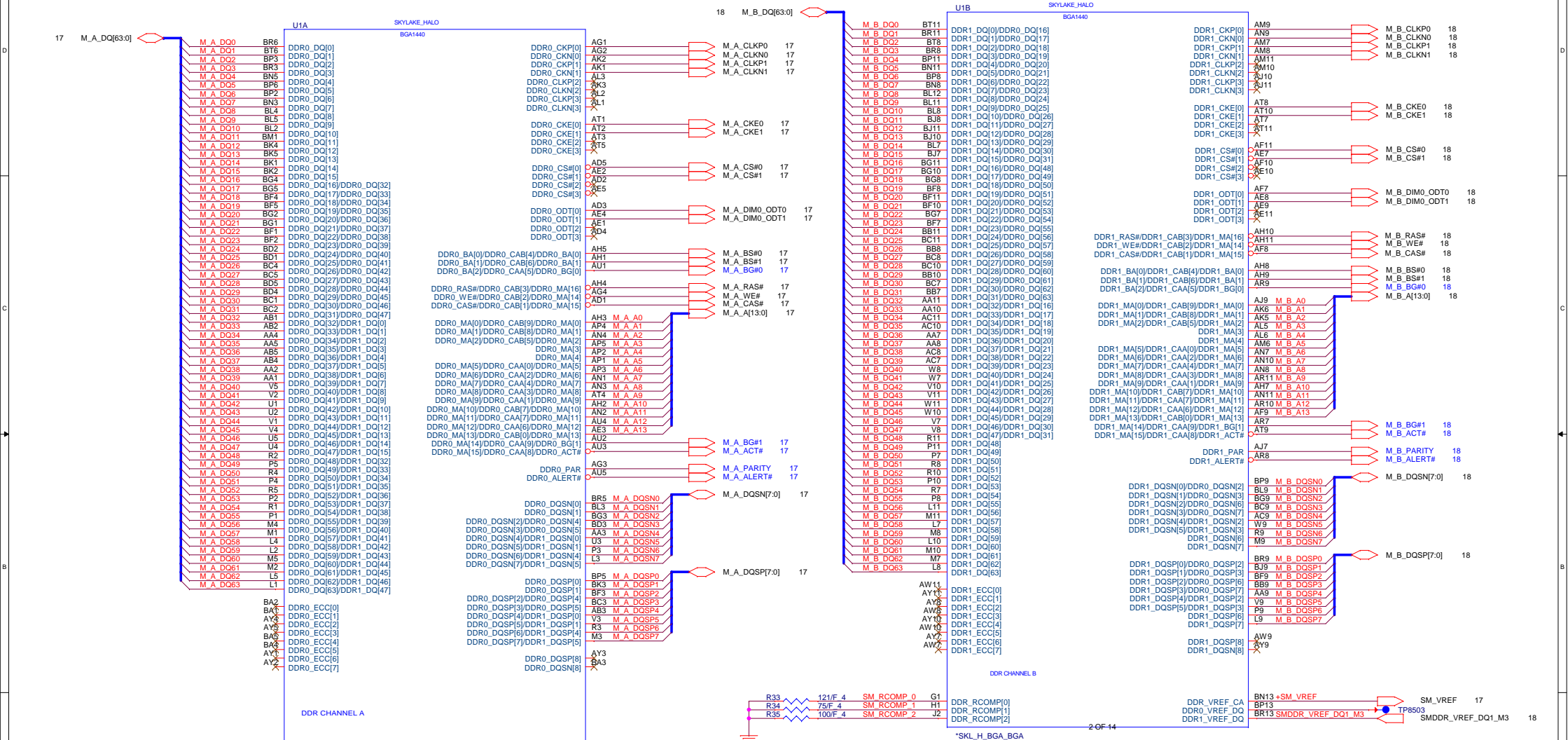


PROJECT : G35
Quanta Computer Inc.

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Date: Thursday, December 24, 2015 1 Sheet 3 of 51

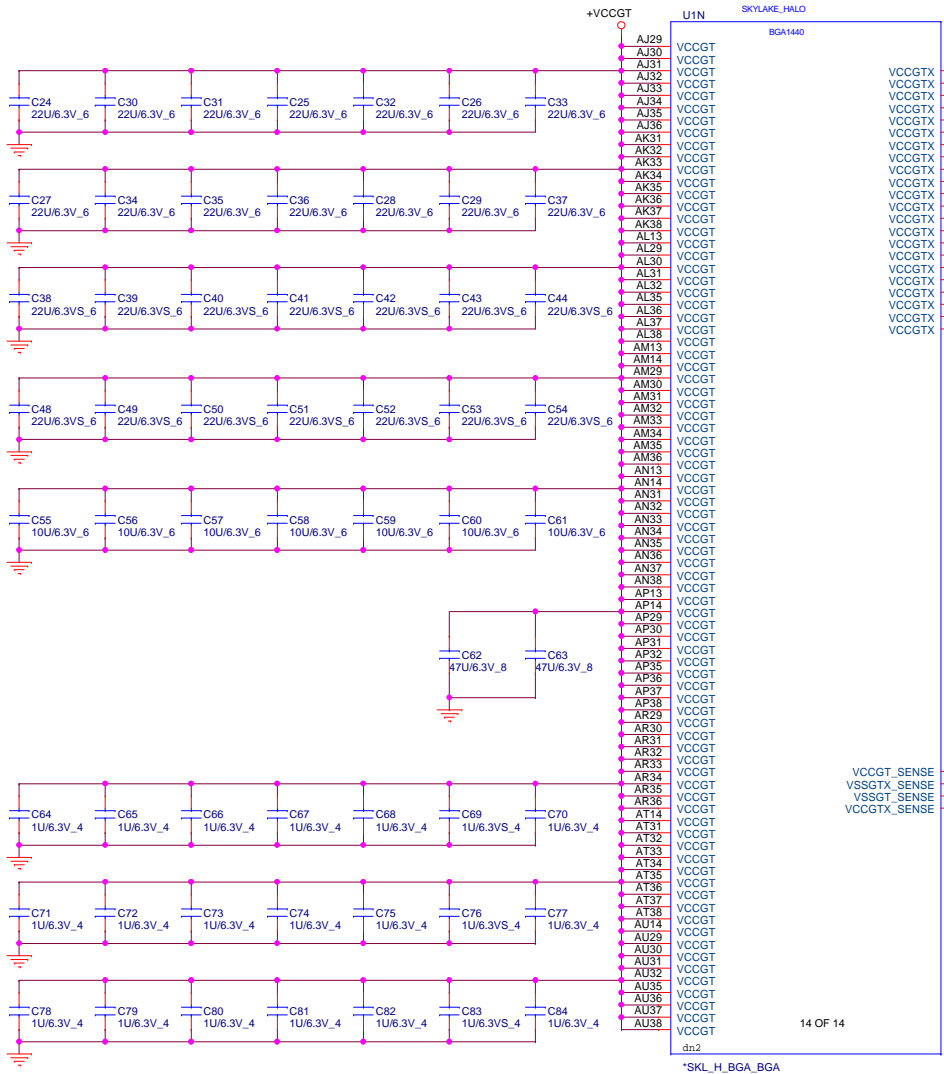
+1.2V/BUS 2,6,10,17,18,42,48,51
+3VSB 10,12,14,16,26,33,37,41,42,46,
+3V 5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,34

SKYLAKE Processor (DDR4)

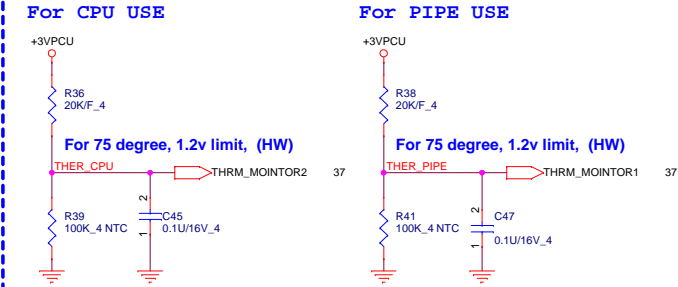


Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

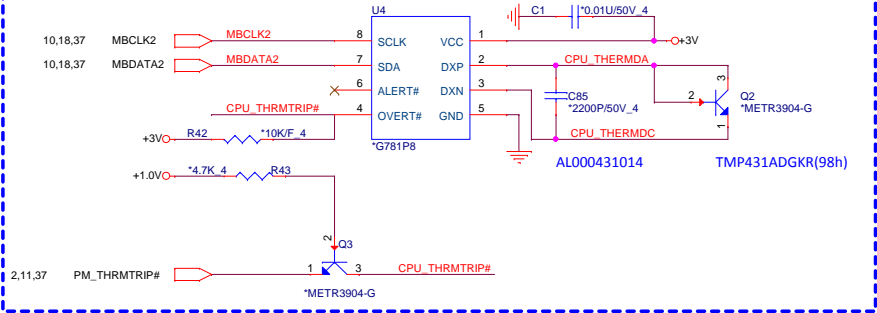
+VCC_CORE 7.43,44
+1.2VSUS 2,6,10,17,18,42,48,51



IO Thrm Protect
Location need thermal confirm

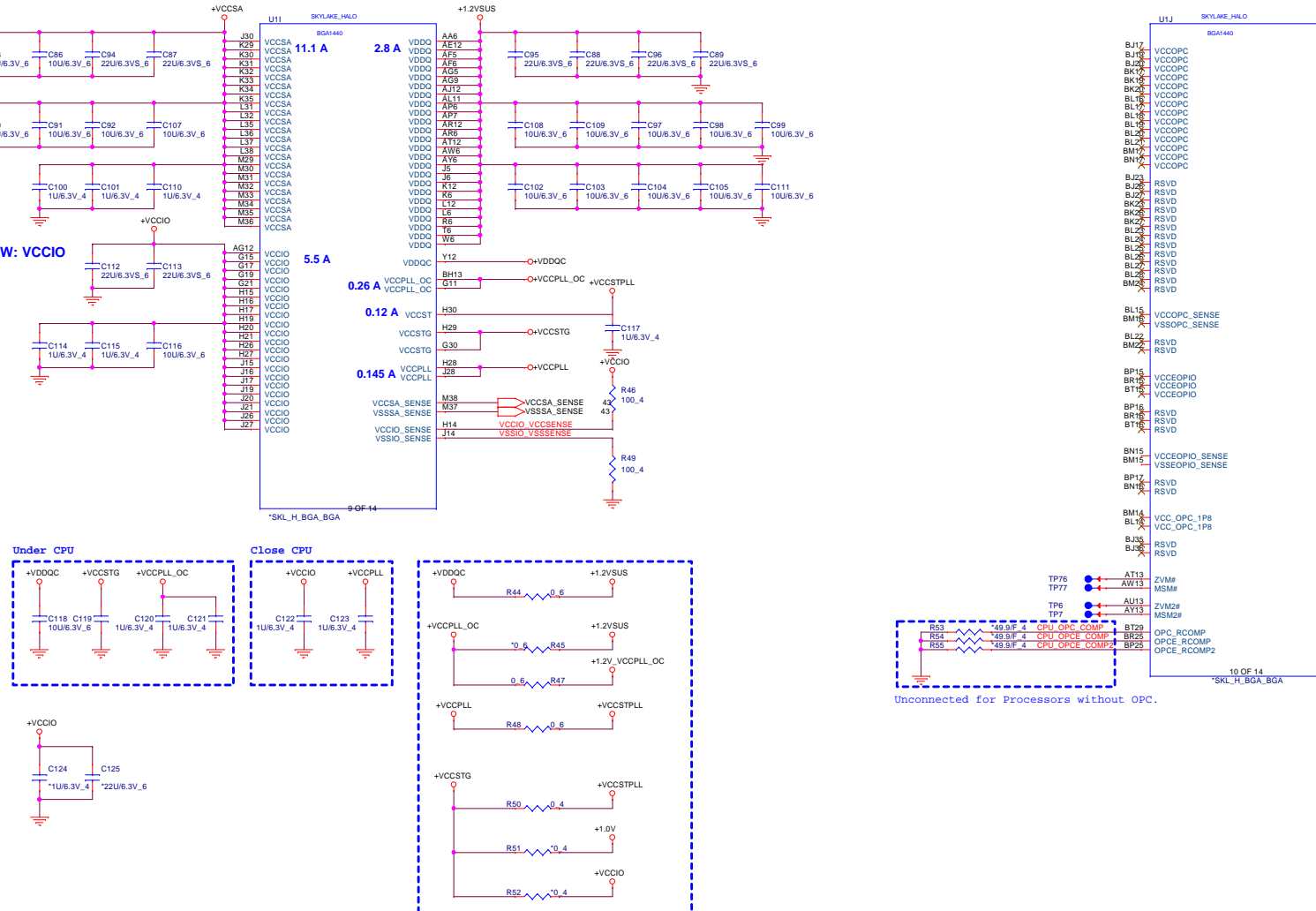


CPU Thermal Sensor
Location need thermal confirm



Follow SKL H EDS page 135 to 45W(GT2): VCCSA=11.1A

Follow SKL H EDS page 135 45W: VDDQ=2.8A

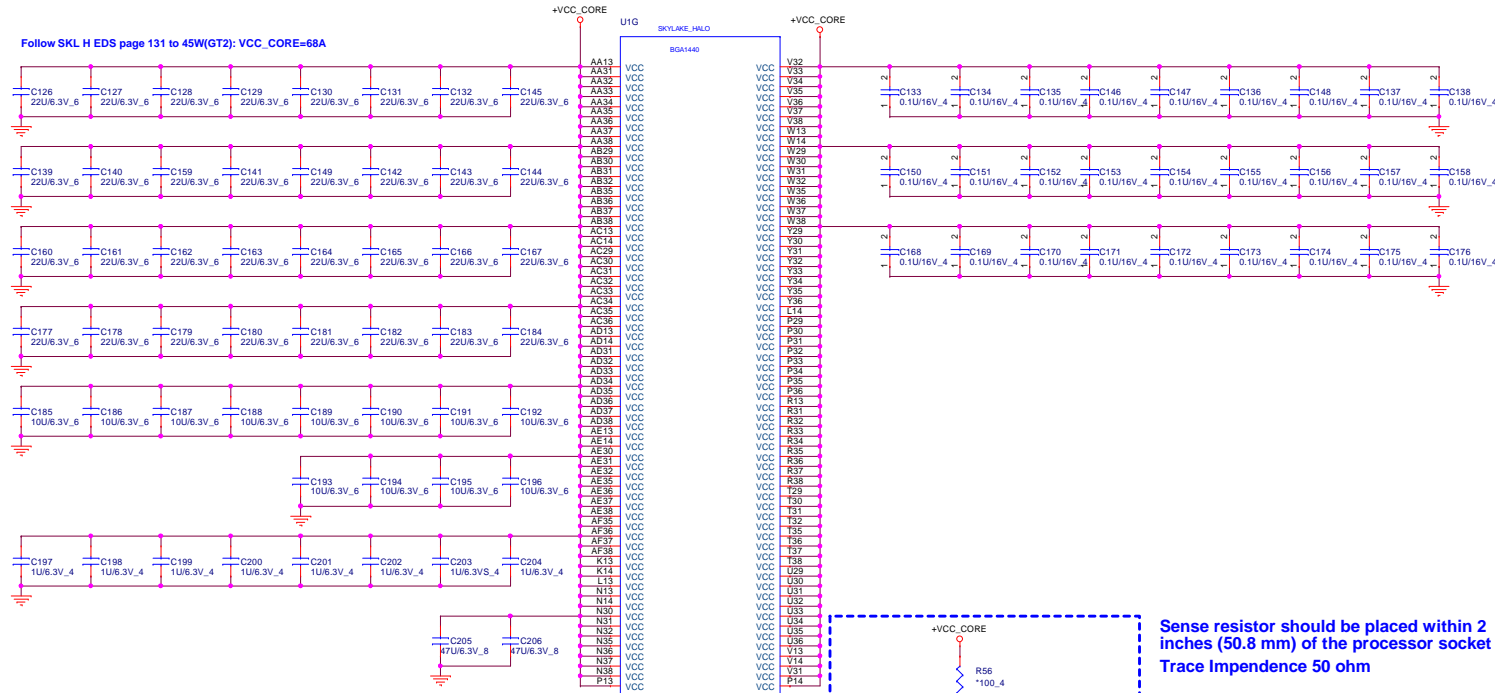
Follow SKL H EDS P136 to 45W: VCCIO
+VCCIO = 0.95V

Unconnected for Processors without OPC.

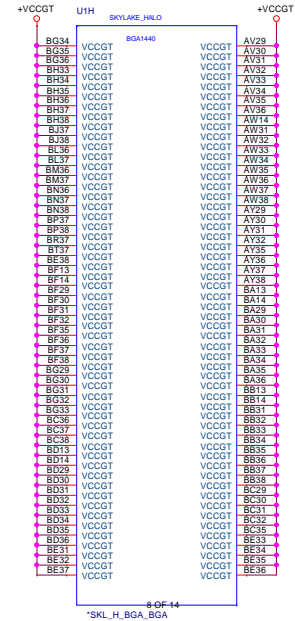


PROJECT : G35
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Follow SKL H DES page 131 to 45W(GT2): VCC_CORE=68A



Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket
Trace Impedance 50 ohm



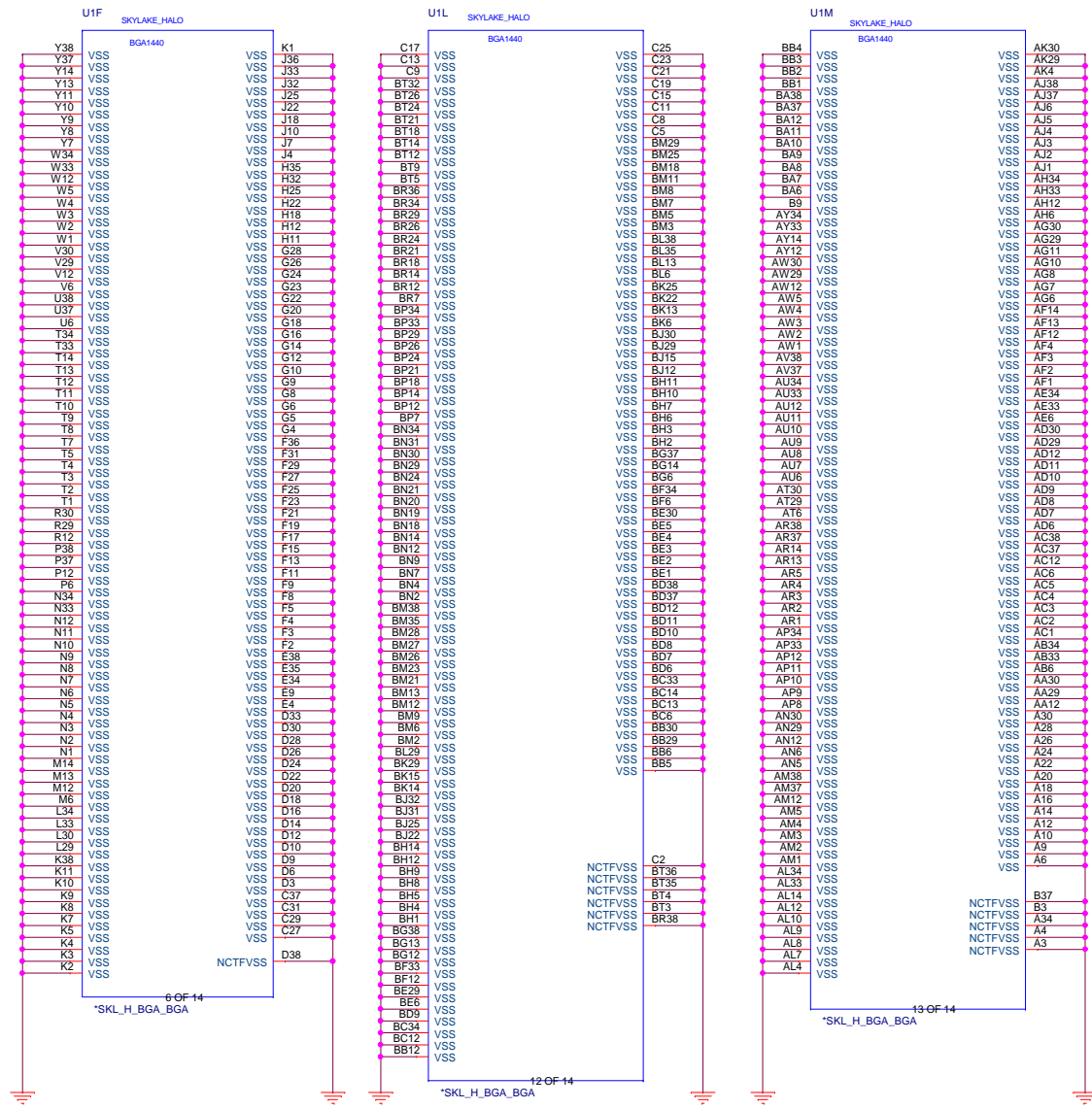
+VCC_CORE 43,44



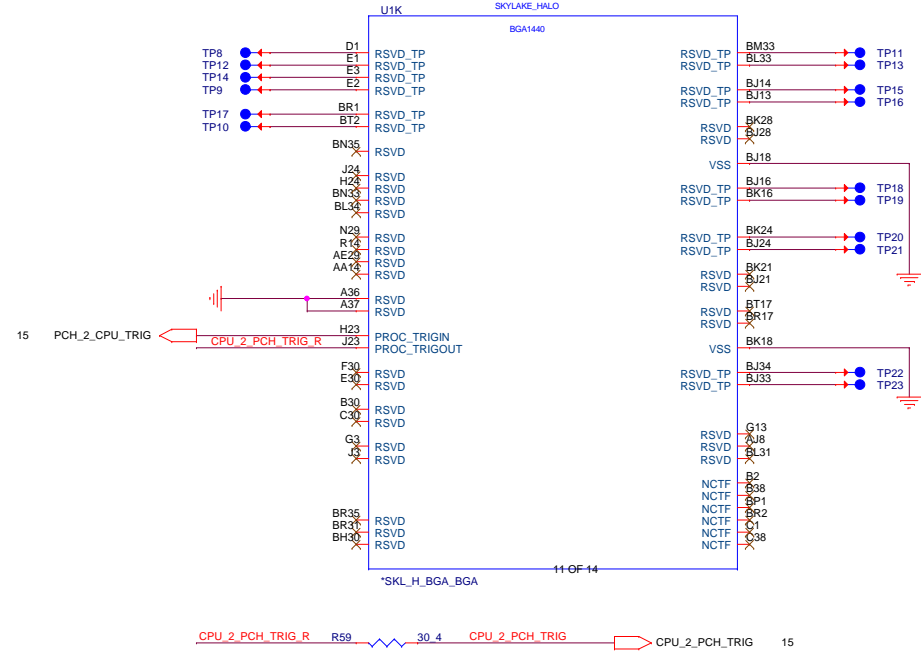
PROJECT : G35
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|--------------------------|-----|
| Custom | 07 - SKL 6/7 (POWER&GND) | 1A |
| Date: Thursday, December 24, 2015 1 Sheet 7 of 51 | | |

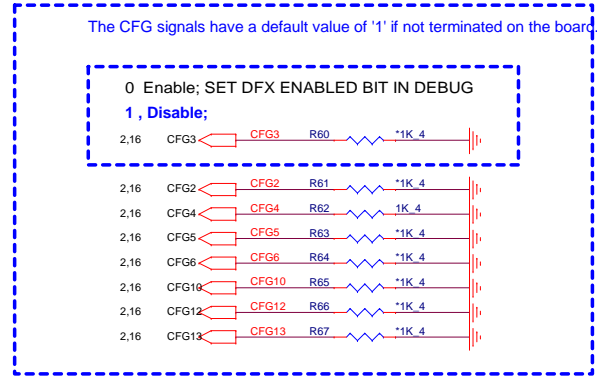
SKL-HProcessor (GND)

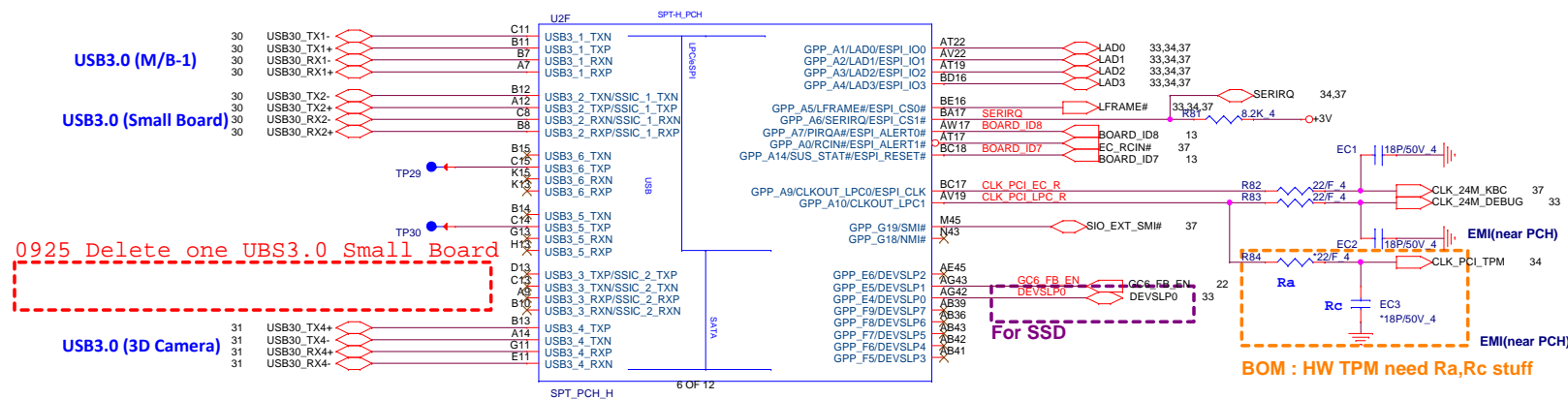
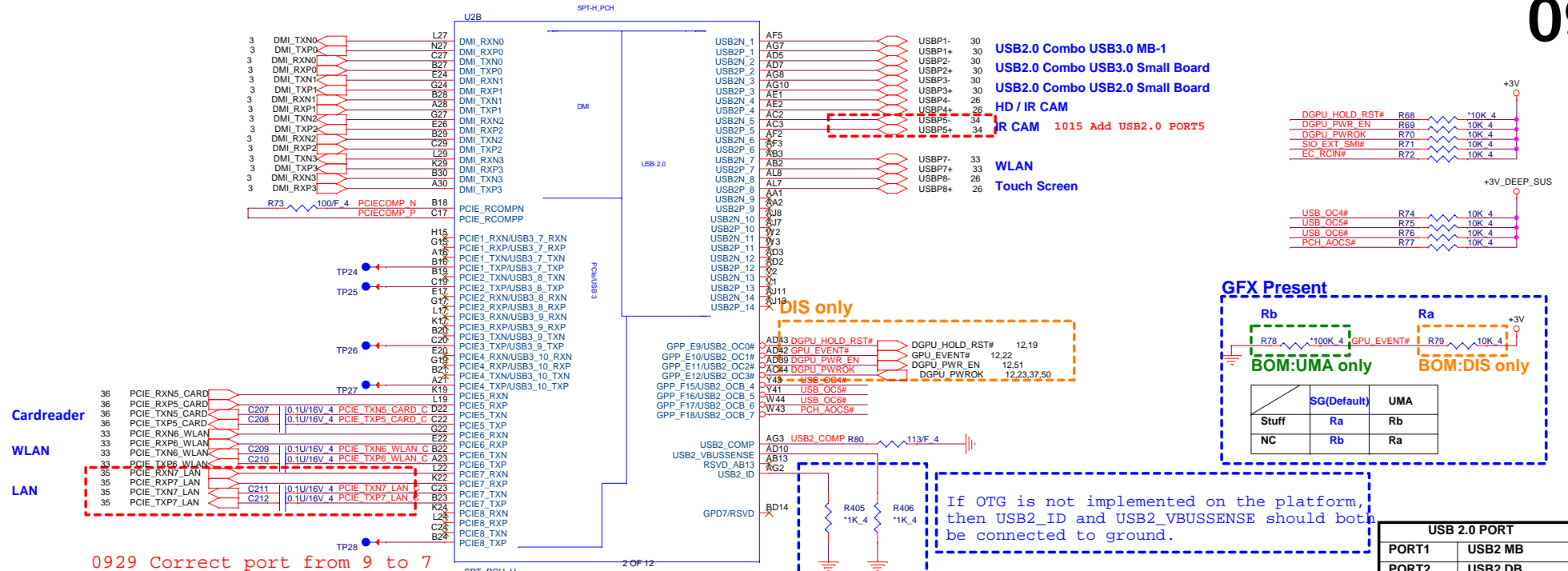


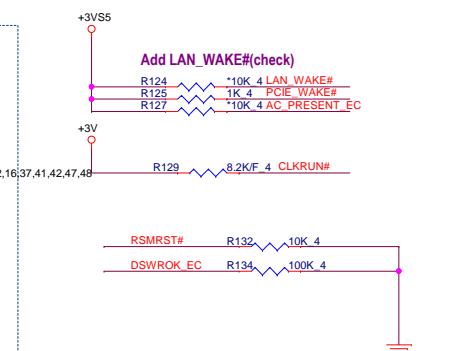
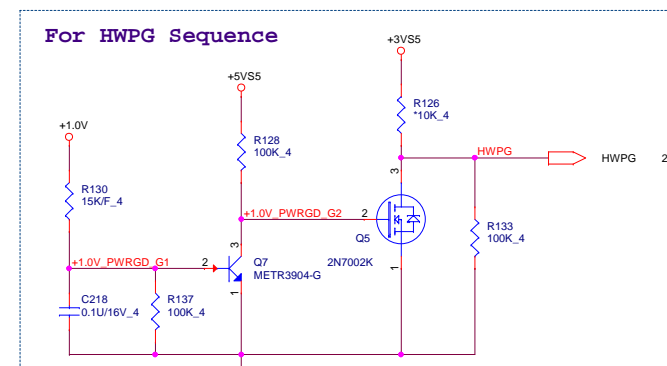
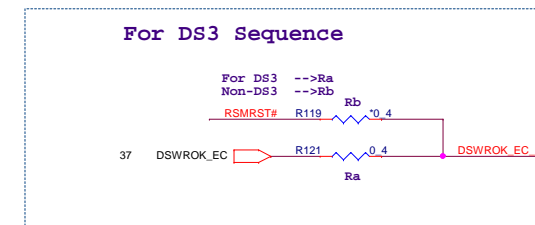
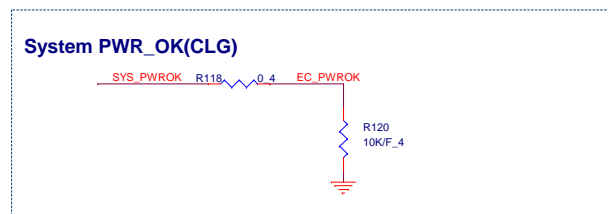
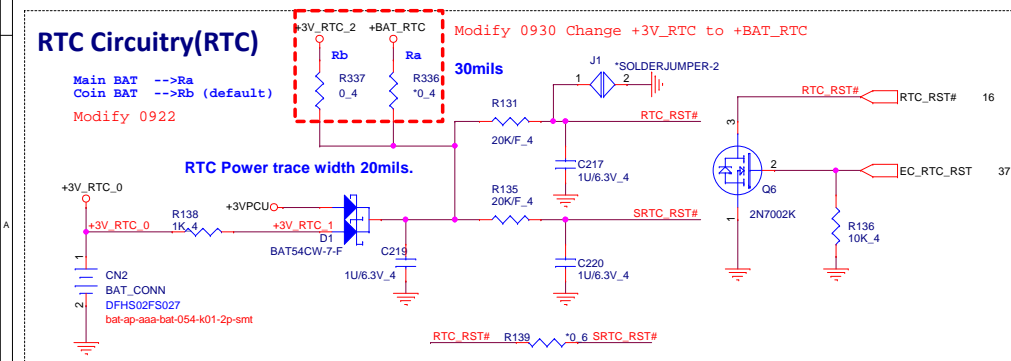
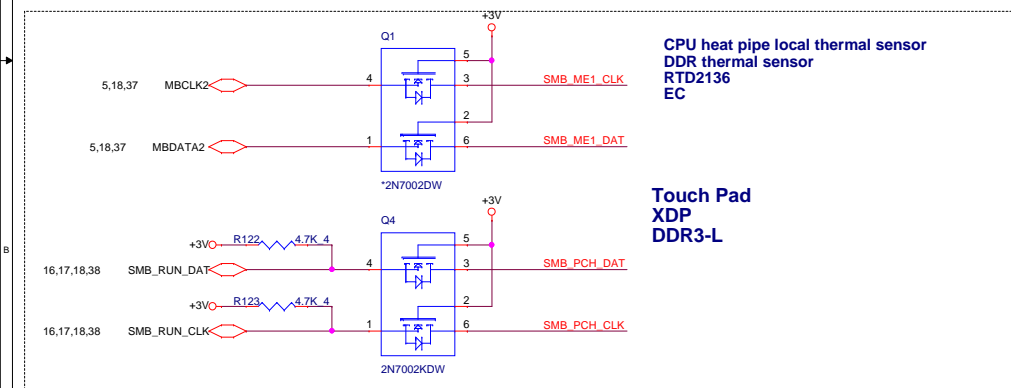
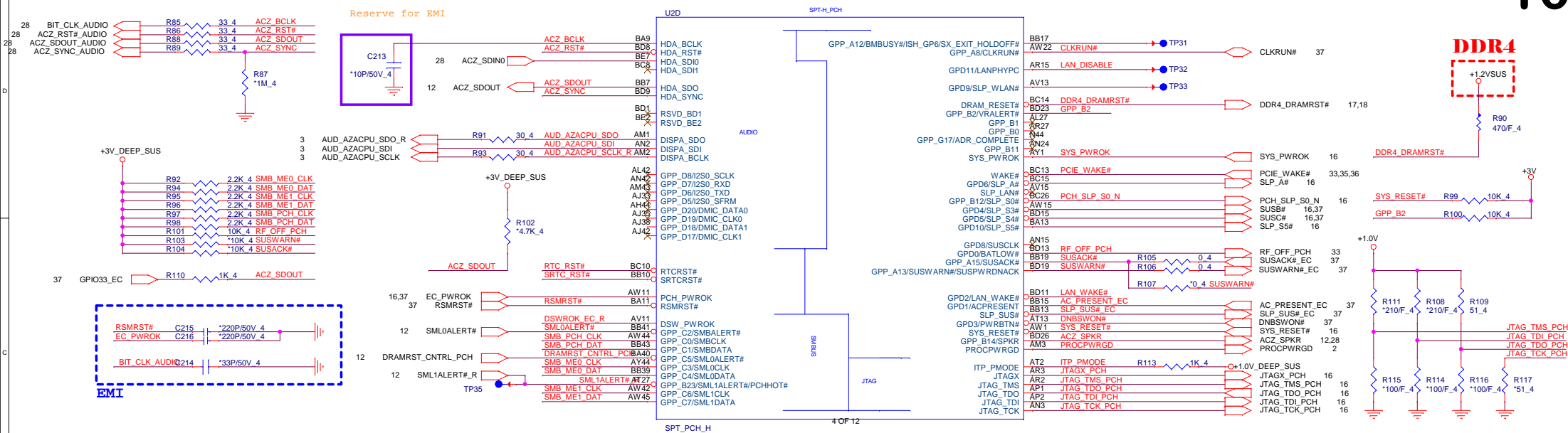
SKL-H Processor (RESERVED, CFG)



Processor Strapping







| HSIO MUX PORT | |
|---------------|--------------|
| PCIE1-4 | NC |
| PCIE5 | Cardreader |
| PCIE6 | Wlan |
| PCIE7 | Lan |
| PCIE8 | NC |
| PCIE9/SATA0A | SSD PCIE * 4 |
| PCIE10 | |
| PCIE11 | |
| PCIE12 | |
| PCIE13 | NC |
| PCIE14 | NC |
| PCIE15 | HDD |
| PCIE16 | NC |
| PCIE17 | NC |
| PCIE18-20 | NC |

SSD PCIE x4 LANE

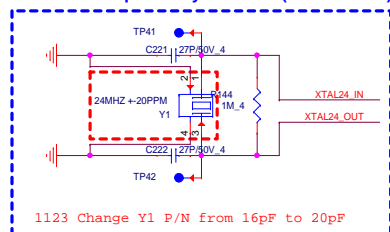
| | | |
|----|-----------------|--|
| 33 | PCIE_SATA_TXP11 | |
| 33 | PCIE_SATA_TXN11 | |
| 33 | PCIE_SATA_RXP11 | |
| 33 | PCIE_SATA_RXN11 | |

Modify 1005 Change HDD SATA Port2 to port1B

HDD1 (SATA1B 6Gb/s)

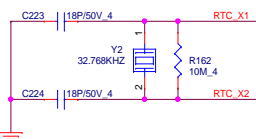
SSD PCIE x4 LANE

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.

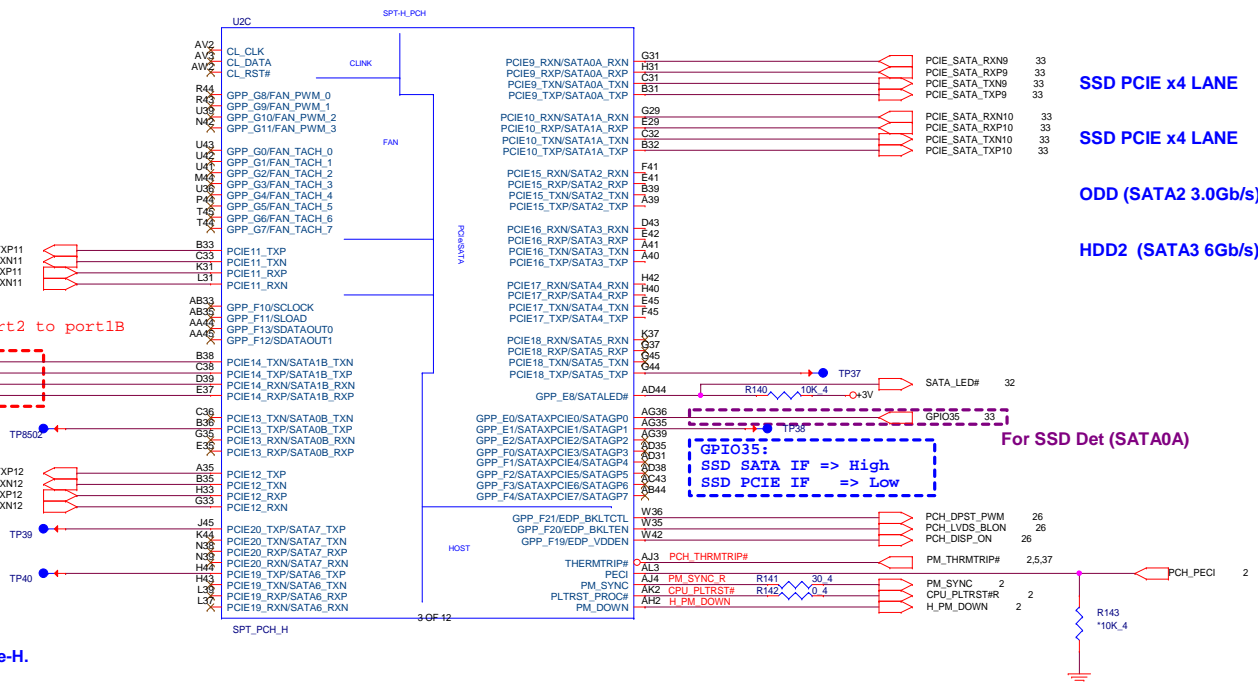


Crystal Components with Surrounding 10 mil Wide Break Out: 4-10 mil Wide GND Shield Trace

RTC Clock 32.768KHz



32.768KHz
BG332768453 CRYSTAL SMD 32.768KHZ(+/-20PPM,12.5PF)
footprint: xtl-3 2X1 5-2 5-0 8h

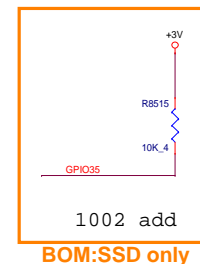


SSD PCIE x4 LANE

SSD PCIE x4 LANE

ODD (SATA2 3.0Gb/s)

HDD2 (SATA3 6Gb/s)



For SSD Det (SATA0A)

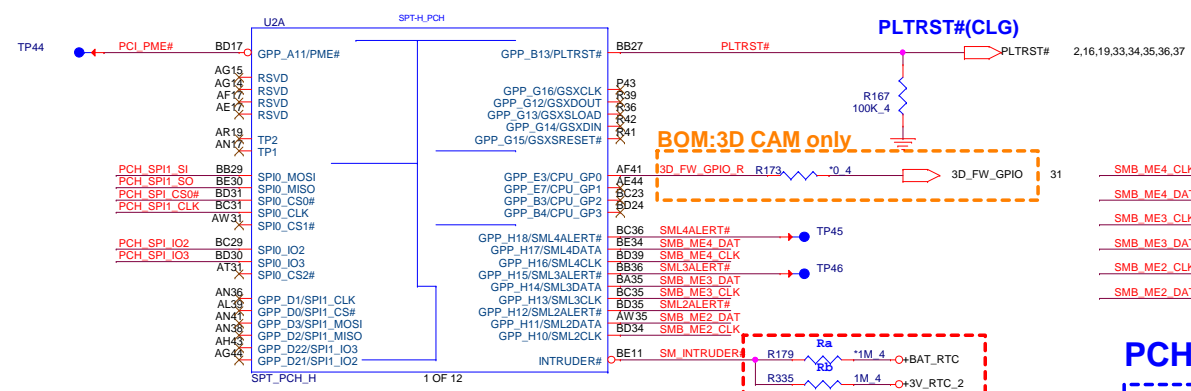
```
GPIO35:
SSD SATA IF => High
SSD PCIE IF  => Low
```

Card Reader

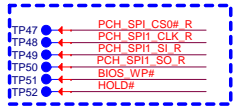
BOM:DIS only

BOM:SSD only

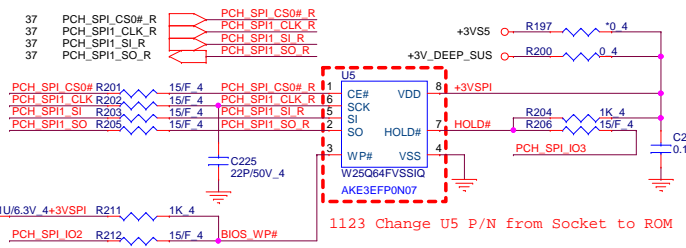
| | | | |
|-------------------|------|--|--------|
| PCIE CLKREQ_WLAN# | R148 | | *10K_4 |
| PCIE CLKREQ_LAN# | R149 | | *10K_4 |
| PCIE CLKREQ_CR# | R151 | | *10K_4 |
| PCIE CLKREQ_VGA# | R152 | | *10K_4 |
| PCIE CLKREQ_0 | R153 | | *10K_4 |
| PCIE CLKREQ_SS0# | R154 | | *10K_4 |
| PCIE CLKREQ_0# | R155 | | *10K_4 |
| PCIE CLKREQ_07# | R156 | | *10K_4 |
| PCIE CLKREQ_08# | R157 | | *10K_4 |
| PCIE CLKREQ_09# | R158 | | *10K_4 |
| PCIE CLKREQ_10# | R159 | | *10K_4 |
| PCIE CLKREQ_11# | R160 | | *10K_4 |
| PCIE CLKREQ_12# | R161 | | *10K_4 |
| PCIE CLKREQ_13# | R163 | | *10K_4 |
| PCIE CLKREQ_14# | R164 | | *10K_4 |
| PCIE CLKREQ_15# | R165 | | *10K_4 |



PCH SPI ROM(CLG)



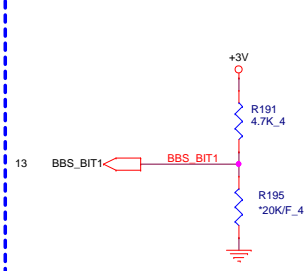
Place to TOP



| Vender | Size | P/N |
|------------|------|-------------------------------|
| EON | 8MB | AKE3EZNOQ01 (EN25QH64-104HIP) |
| Winbond | 8MB | AKE3EFFP0N07 (W25Q64FVSSIQ) |
| GigaDevice | 8MB | AKE3EGNOQ01 (GD25B64BSIGR) |
| Socket | | DFHS08FS023 |

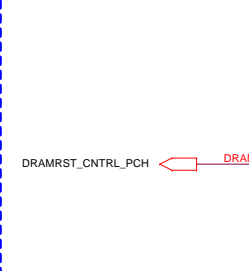
NO REBOOT IF SAMPLED HIGH

HIGH:TOP SWAP ENABLED (CRB)
LOW: Disable "No Reboot" mode. (Default)



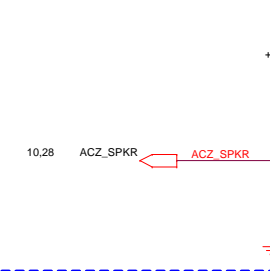
ESPI/LPC SELECT STRAP

HIGH:ESPI Is selected for EC.
LOW: LPC Is selected for EC. (Default)



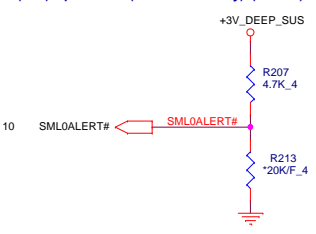
TOP SWAP OVERRIDE STRAP

HIGH:TOP SWAP ENABLED (CRB)
LOW:TOP SWAP DISABLED(DEFAULT)



TLS CONFIDENTIALITY ENABLED

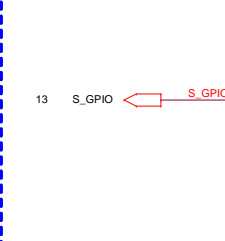
HIGH:T Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)
LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)



PCH Strap Pin

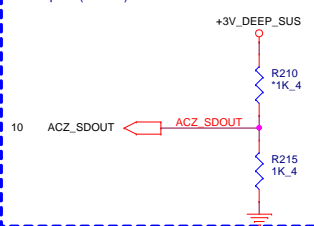
BOOT SELECT STRAP

HIGH:LPC
LOW: SPI. (Default)



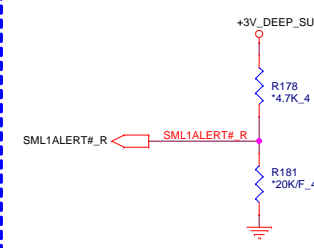
TLS CONFIDENTIALITY ENABLED

HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. (CRB)
LOW: security measures defined in the Flash Descriptor. (Default)



RESERVED

This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.



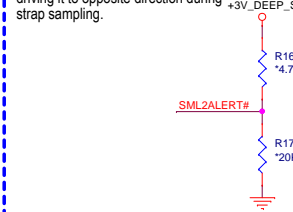
RESERVED

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



ESPI FLASH SHARING MODE

HIGH:SLAVE ATTACHEHD FLASH SHARING
LOW: 0: MASTER ATTACHED FLASH SHARING
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.



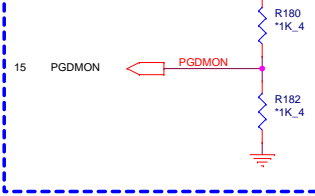
RESERVED

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



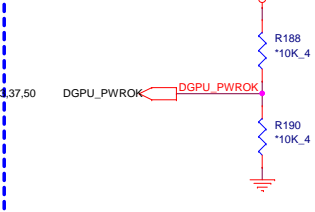
DFX TEST MODE QUALIFIER FOR OTHER DFX STRAP WHEN SAMPLED LOW

15 PGDMON



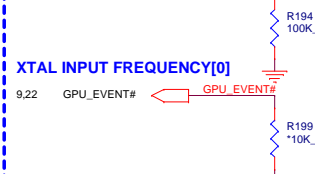
DFX TEST MODE

XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL



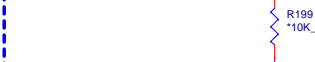
RING OSCILLATOR BYPASS

DGPU_HOLD_RST#



XTAL INPUT FREQUENCY[0]

GPU_EVENT#



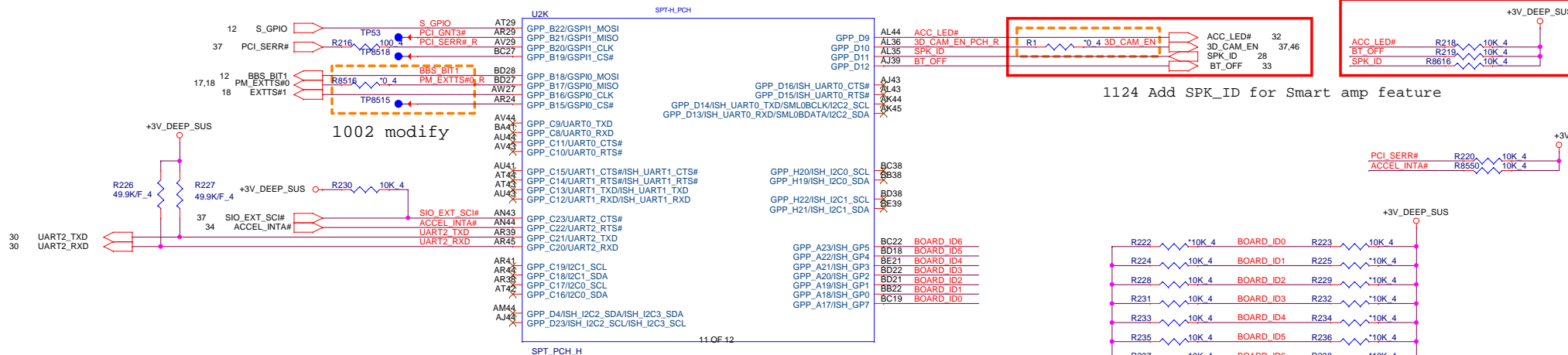
XTAL INPUT FREQUENCY[1]

DGPU_PWR_EN

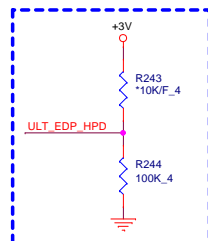


PROJECT : G35
Quanta Computer Inc.

| | | |
|--|---|--------|
| Size Custom | Document Number 12 -- PCH 4/7 (GPIO/MISC) | Rev 1A |
| Date: Thursday, December 24, 2015 Sheet 12 of 51 | | |

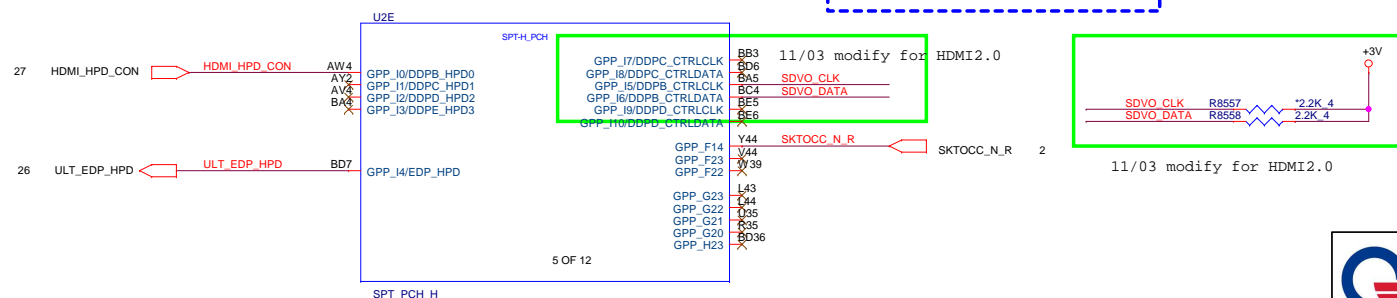


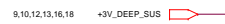
Reserve EDP HPD opposites circuit!

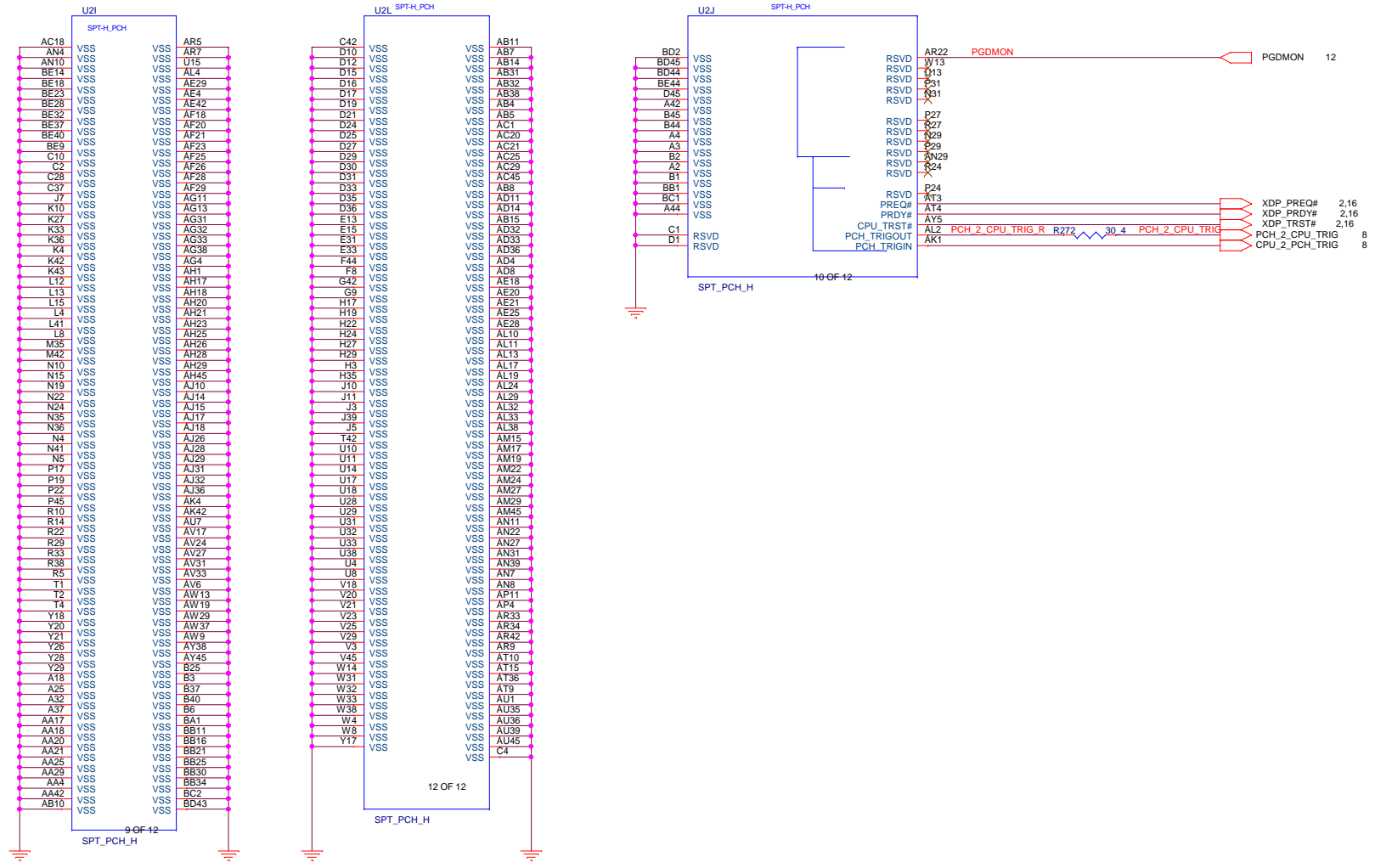


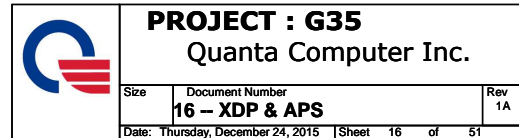
| Model | BOARD_ID[8:7] ID8;ID7 | BOARD_ID[6:5] ID6;ID5 | Board ID [4:3] ID4;ID3 | BOARD_ID[2:1] ID2;ID1 | BOARD_ID0 ID0 |
|------------|----------------------------|--------------------------|---------------------------|-------------------------------|--------------------|
| Definition | 00 Non 3D SKU 01 3D SKU | 00 Reserve | 00 Reserve | 00 15" 01 17" 10 17" SP | 0 : UMA 1 : DIS |

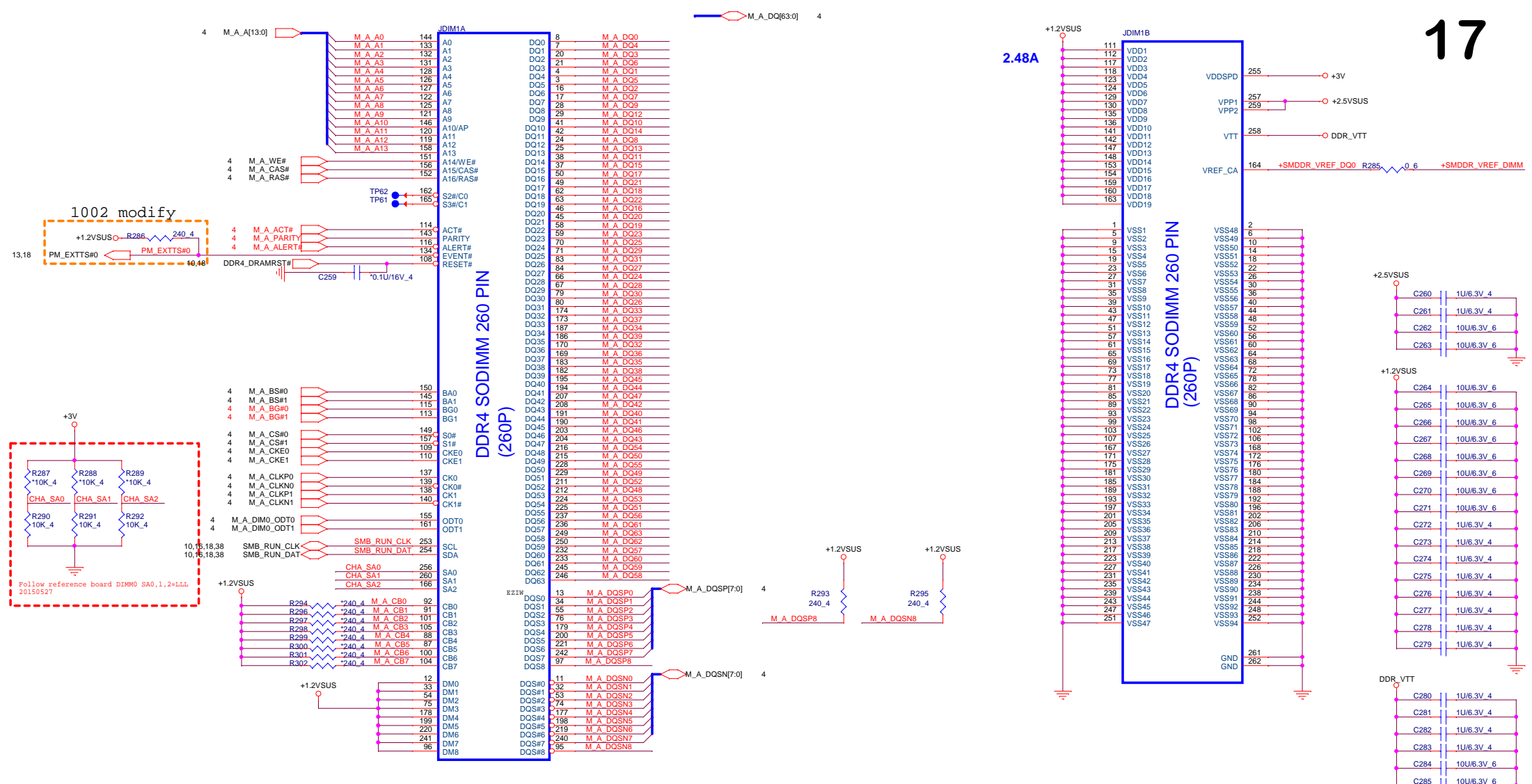
- This signal has a weak internal pull-down.
- 0 = Port C and D is not detected.
- 1 = Port C and D is detected.





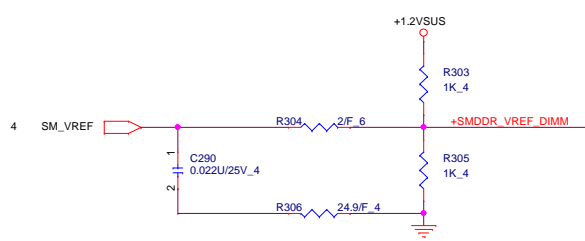
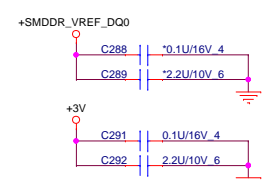







Place these Caps near So-Dimm0.

0923 Del C286 C287



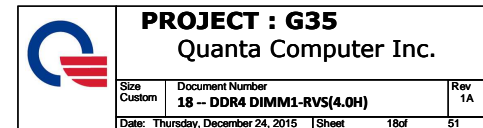
Place these Caps near So-Dimm0.

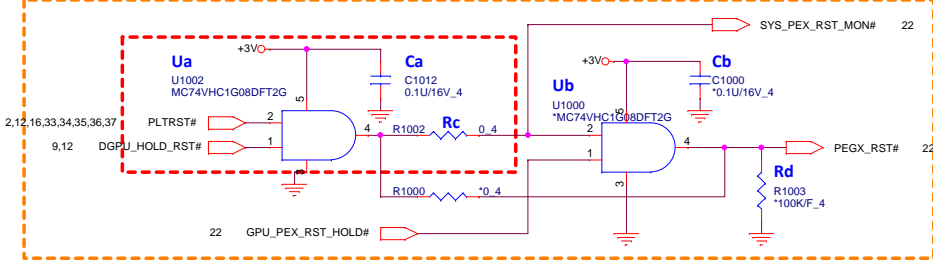
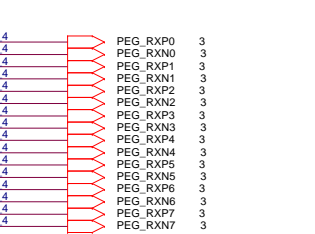
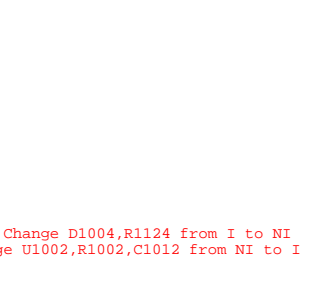
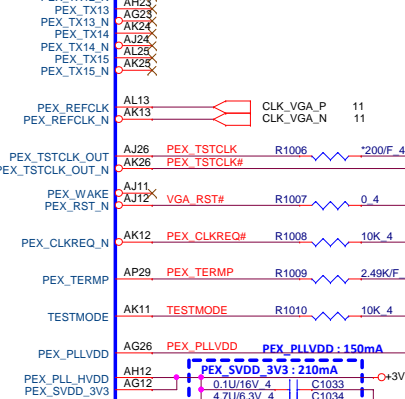
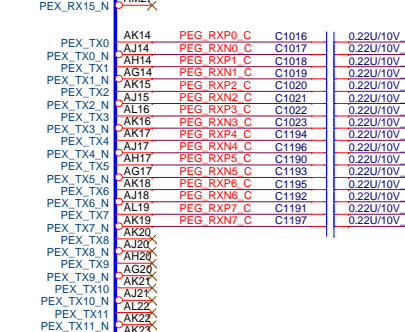
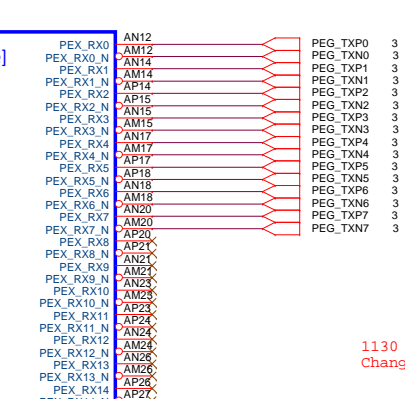
1uF/10uF 4pcs on each side of connector



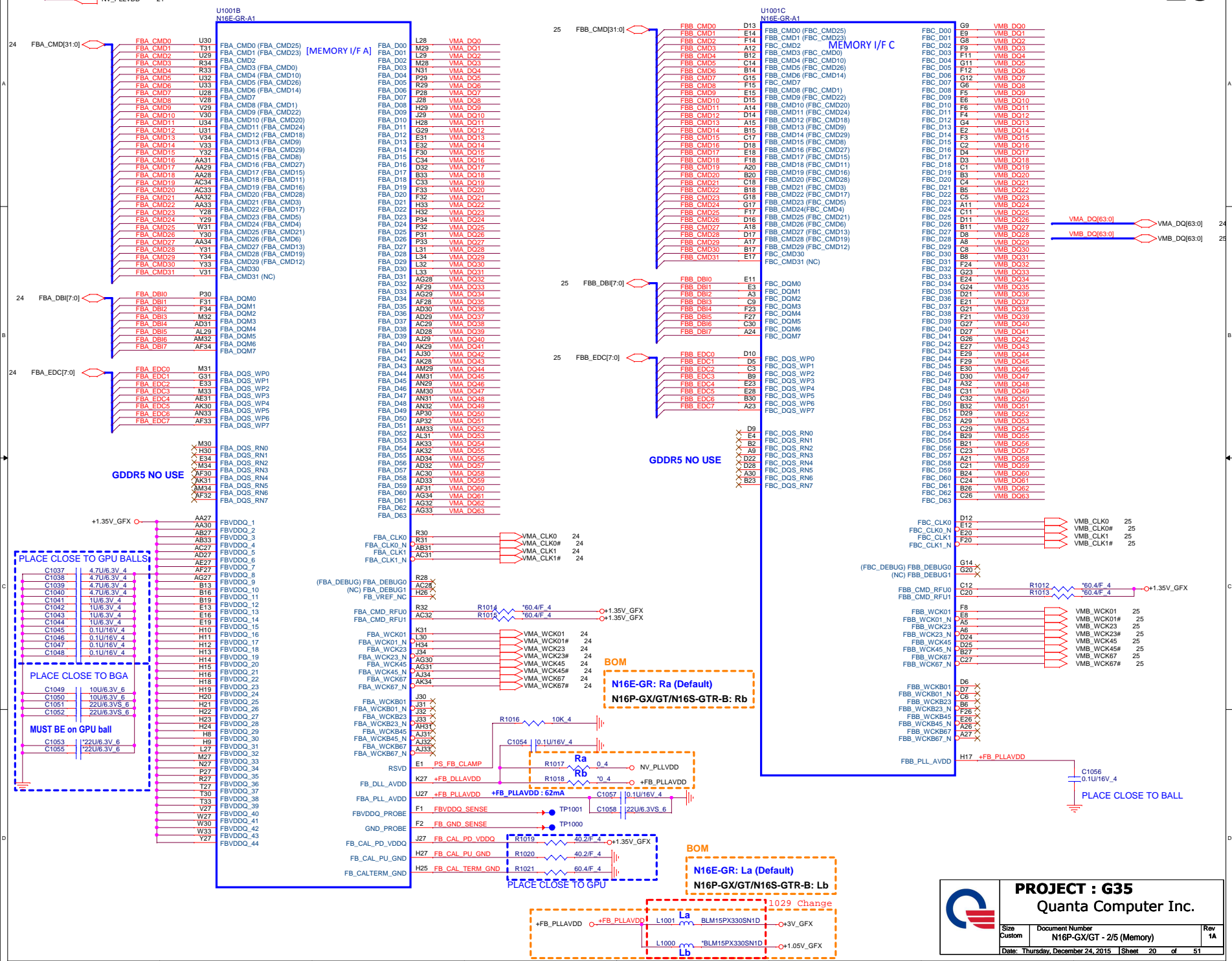
PROJECT : G35
Quanta Computer Inc.

| | | |
|---|---|-----------|
| Size Custom | Document Number 17 - DDR4 DIMM0-STD(4.0H) | Rev 1A |
| Date: Thursday, December 24, 2015 Sheet 17of 51 | | |

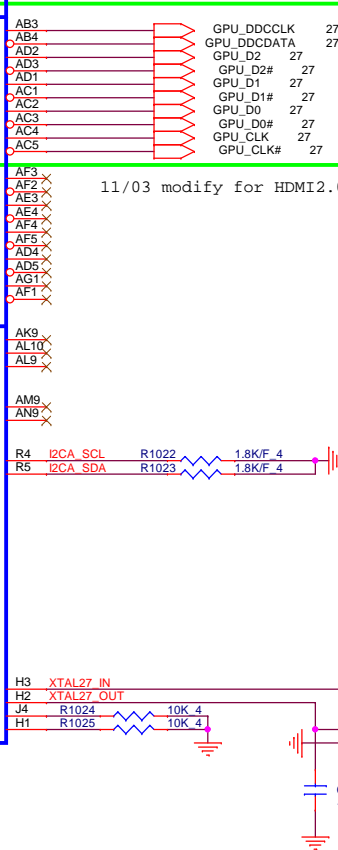
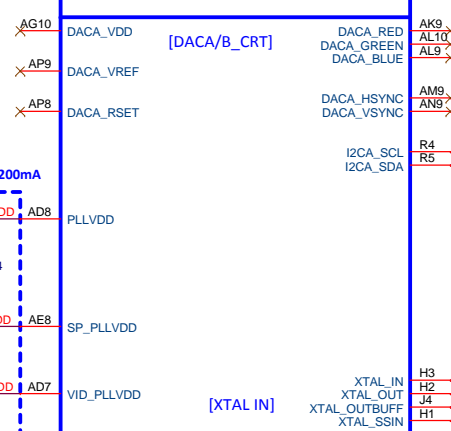
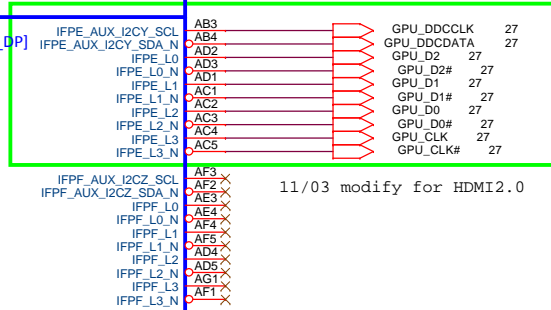
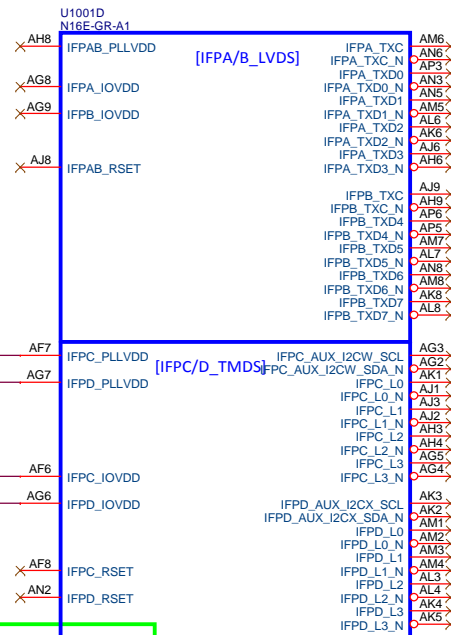
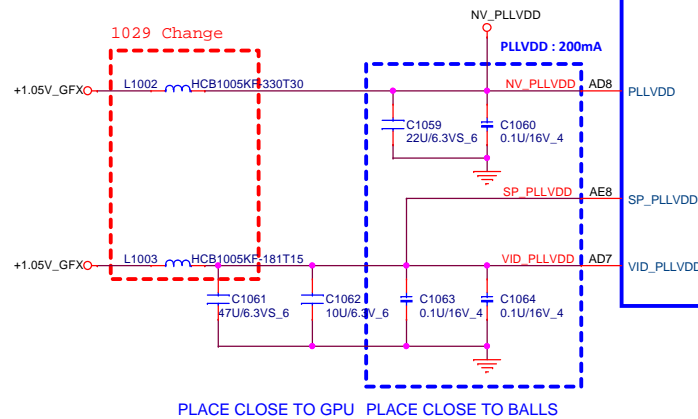
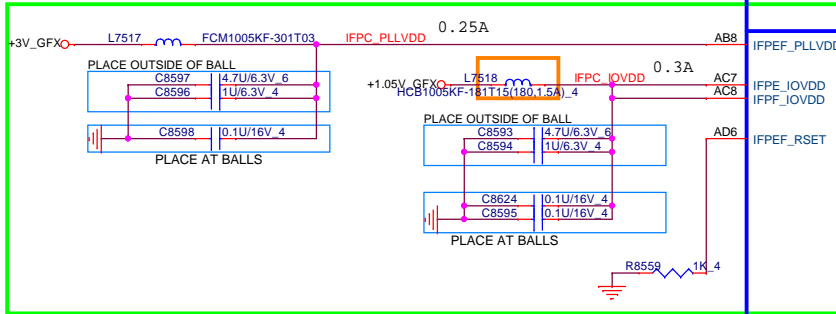
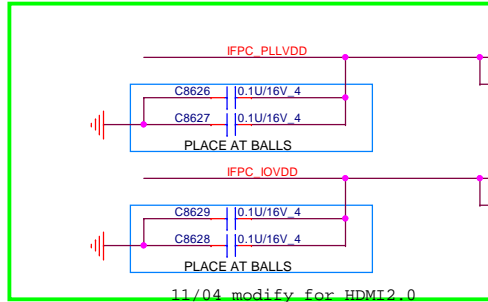




| GPU type | Part Number | Part Description | Where Used |
|----------|-------------|------------------------------------|-------------|
| N16P-GT | AJ0N16P0T05 | IC CTRL(908P)N16P-GT-A2(BGA)TOPBSQ | G35A |
| | AJ0N16P0T06 | IC CTRL(908P)N16P-GT-A2(BGA)QBCON | |
| N16P-GX | AJ0N16P0T14 | IC CTRL(908P)N16P-GX-A2(BGA)TOPBSQ | G35A / G37A |
| | AJ0N16P0T15 | IC CTRL(908P)N16P-GX-A2(BGA)QBCON | |
| N16E-GR | AJ0N16E0T02 | IC CTRL(908P)N16E-GR-A1(BGA)TOPBSQ | G35A / G37A |
| | AJ0N16E0T03 | IC CTRL(908P)N16E-GR-A1(BGA)QBCON | |

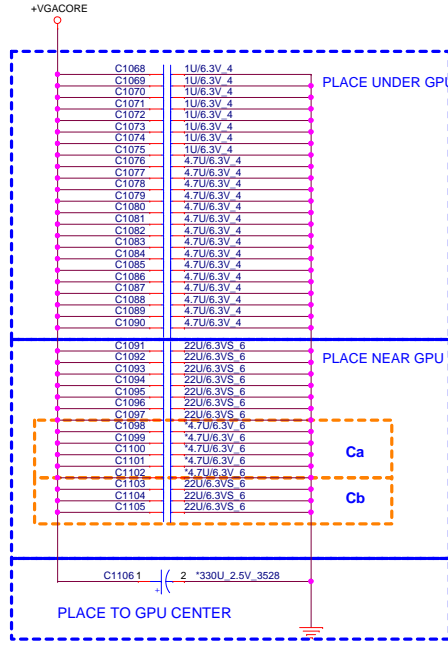
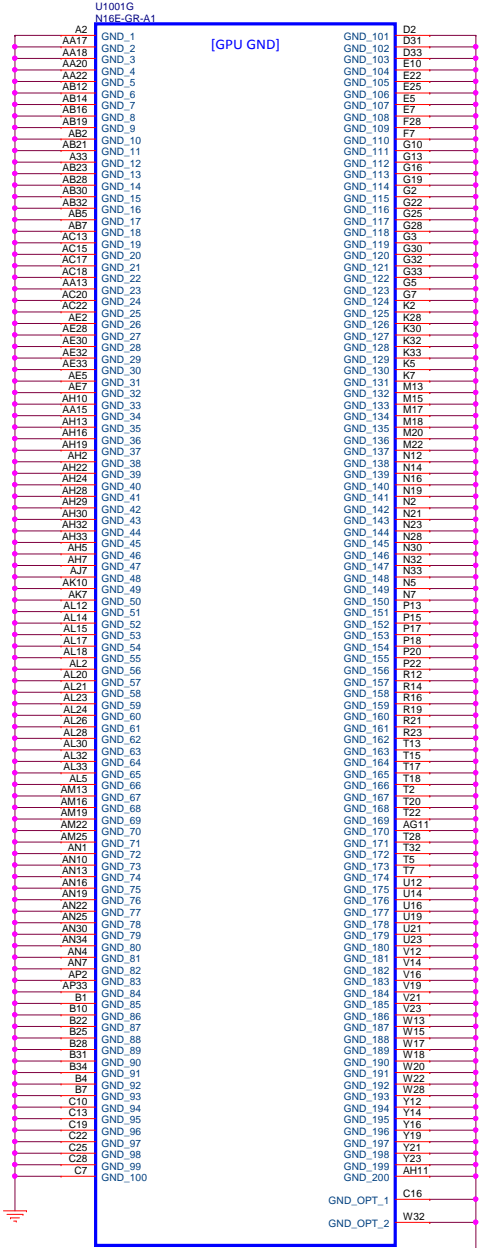
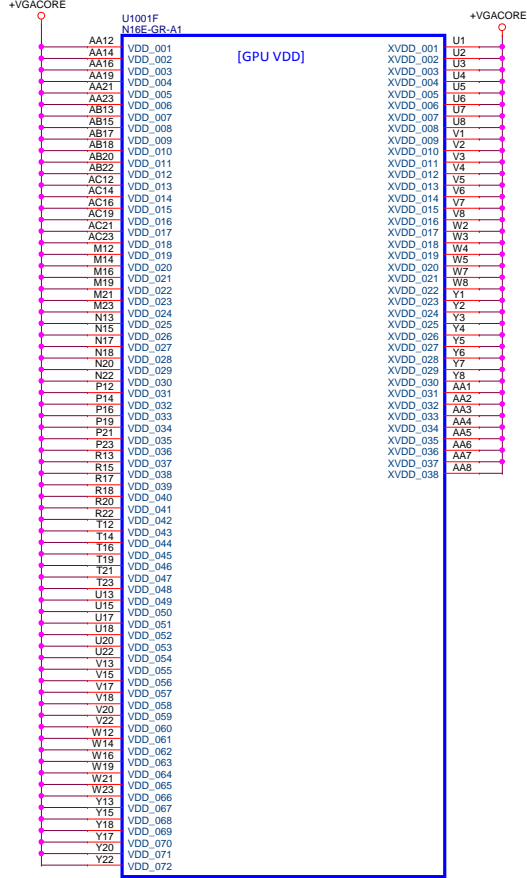


+1.05V_GFX 19.20.23.51
NV_PLLVDD 20



| | |
|------------|-------------------|
| +3V_AON | 19,22,27,51 |
| +3V_GFX | 19,20,21,22,49,51 |
| +1.35V_GFX | 20,24,25,50 |
| +1.05V_GFX | 19,20,21,51 |
| +VGACORE | 49 |

VDD/XVDD : 62A



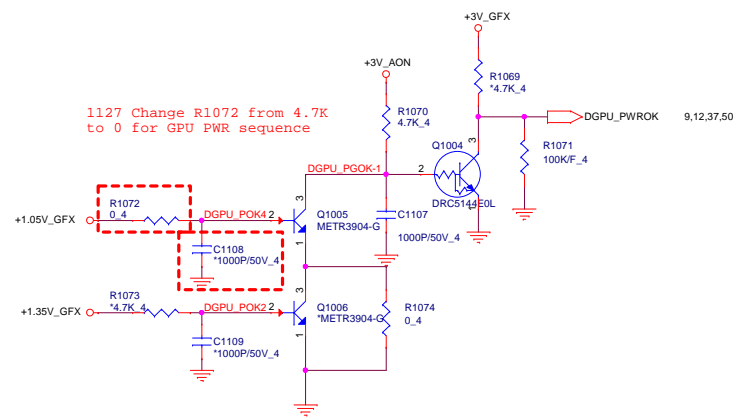
GPU BOM:

N16E-GR: Ca Unstuff, Cb Stuff (Default)

N16P-GX/GT/N16S-GTR-B: Ca change 4.7u stuff , Cb unstuff

4.7 uF : CH5471K9E07 CAP CHIP
4.7U 6.3V(+10%,X5R,0603)

For meet Power down sequence for +3V_GFX



CHANNEL A: 2G/4G GDDR5

+1.35V_GFX 20,23,25,50

20 VMA_DQ[63:0] VMA_DQ[63:0]
 20 FBA_CMD[31:0] FBA_CMD[31:0]
 20 FBA_DBI[7:0] FBA_DBI[7:0]
 20 FBA_EDC[7:0] FBA_EDC[7:0]

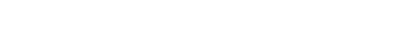
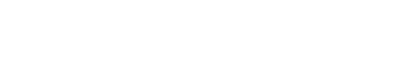
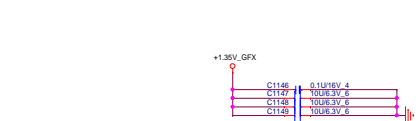
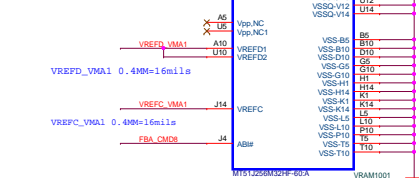
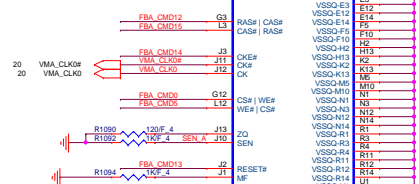
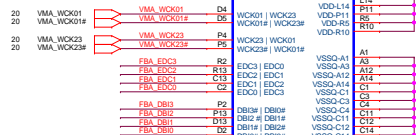
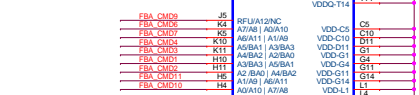
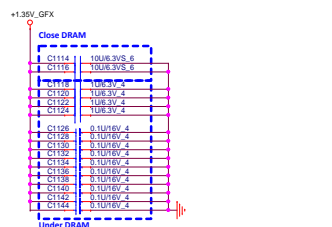
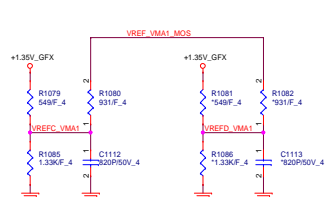
MF=0 Non-mirrored

QD24~31

QD16~23

QD8~15

QD0~7



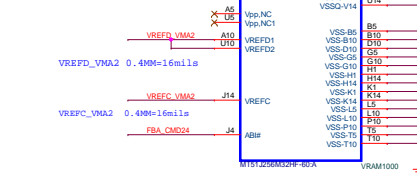
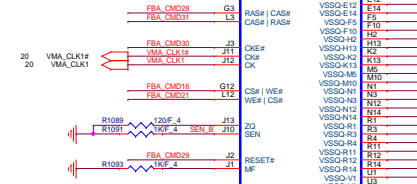
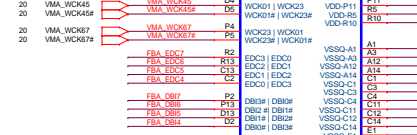
MF=0 Non-mirrored

QD56~63

QD48~55

QD40~47

QD32~39



GDDR5 Mode H Mapping

< 0-31 > < 32-63 > Memory

| | | |
|-------|-------|---------|
| CHD0 | CHD16 | CS* |
| CHD1 | CHD17 | A3_BA3 |
| CHD2 | CHD18 | A2_BA0 |
| CHD3 | CHD19 | A4_BA2 |
| CHD4 | CHD20 | A5_BA1 |
| CHD5 | CHD21 | WE* |
| CHD6 | CHD22 | A7_A8 |
| CHD7 | CHD23 | A6_A11 |
| CHD8 | CHD24 | AB1* |
| CHD9 | CHD25 | A12_RPU |
| CHD10 | CHD26 | A0_A10 |
| CHD11 | CHD27 | A1_A9 |
| CHD12 | CHD28 | RAS* |
| CHD13 | CHD29 | RST* |
| CHD14 | CHD30 | CKE* |
| CHD15 | CHD31 | CAS* |

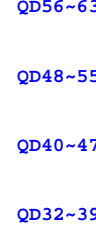
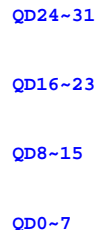


PROJECT : G35
 Quanta Computer Inc.

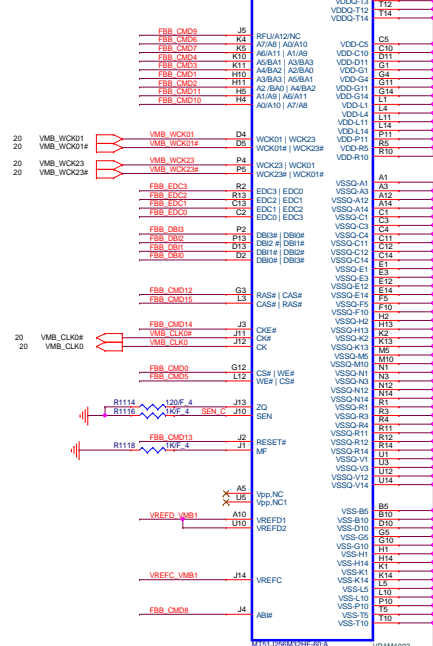
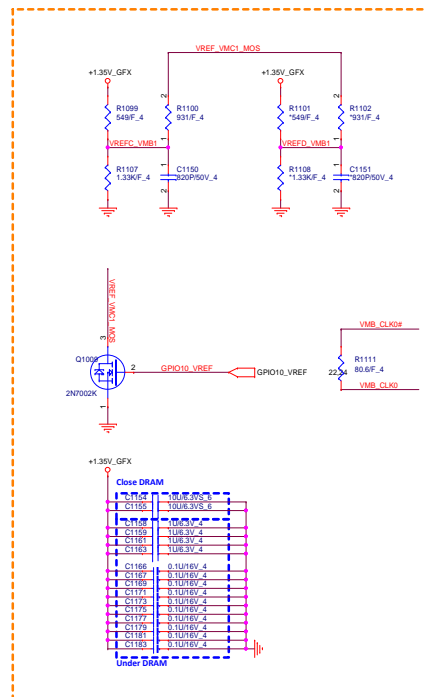
Rev
 14
 Thursday, November 24, 2016 10:00 AM

N16S-GTR-B: unstuff VRAM
N16P-GX/GT/N16E-GR: stuff VRAM (Default)

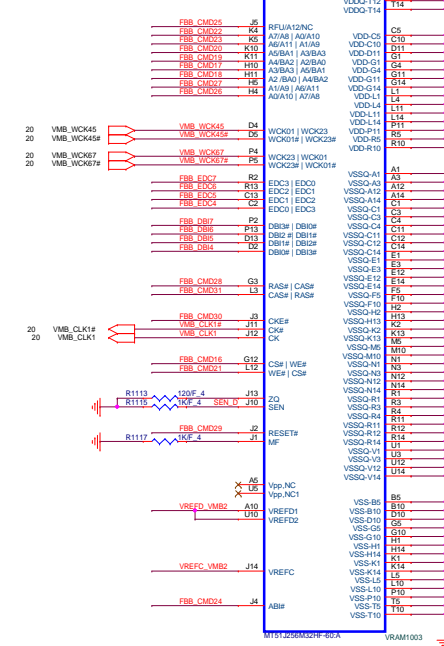
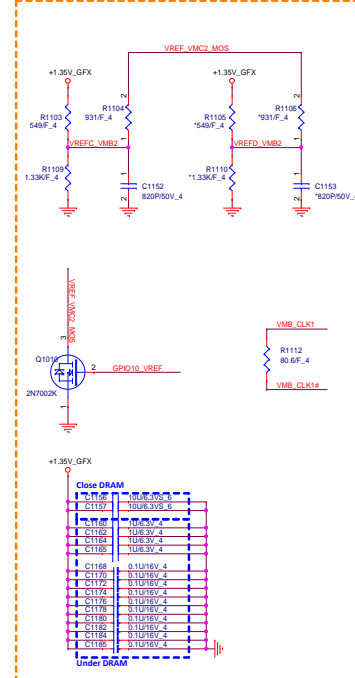
MF=0 Non-mirrored



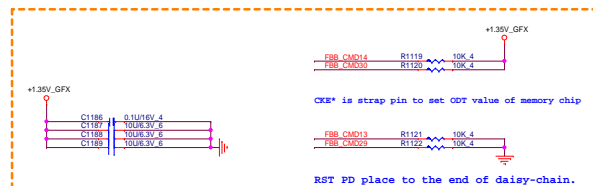
N16S-GTR-B: unstuff VRAM
N16P-GX/GT/N16E-GR: stuff VRAM (Default)



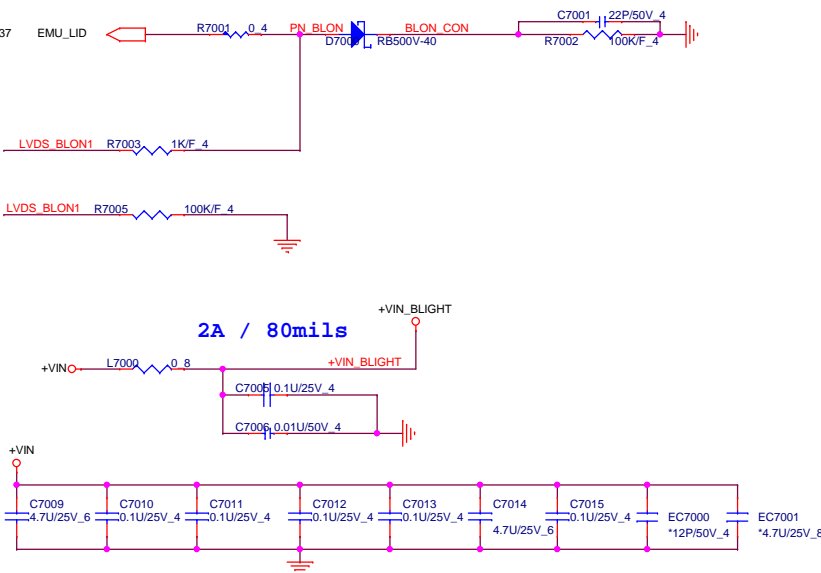
N16S-GTR-B: unstuff VRAM
N16P-GX/GT/N16E-GR: stuff VRAM (Default)



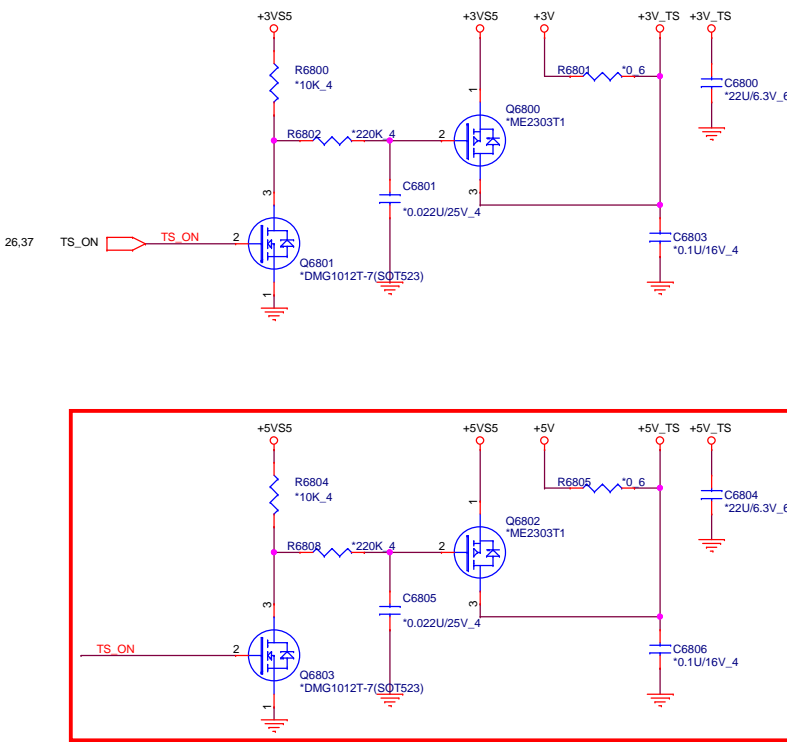
| GDDR5 Mode H Mapping | | |
|----------------------|---------|---------|
| < 0-31 | > 32-63 | Memory |
| CM0 | CM16 | CS* |
| CM1 | CM17 | A3_BA3 |
| CM2 | CM18 | A2_BA0 |
| CM3 | CM19 | A4_BA2 |
| CM4 | CM20 | A5_BA1 |
| CM5 | CM21 | WE* |
| CM6 | CM22 | A7_A8 |
| CM7 | CM23 | A6_A11 |
| CM8 | CM24 | AB1* |
| CM9 | CM25 | A12_RFU |
| CM10 | CM26 | A0_A10 |
| CM11 | CM27 | A1_A9 |
| CM12 | CM28 | RAS* |
| CM13 | CM29 | RST* |
| CM14 | CM30 | CKE* |
| CM15 | CM31 | CAS* |



LID Switch



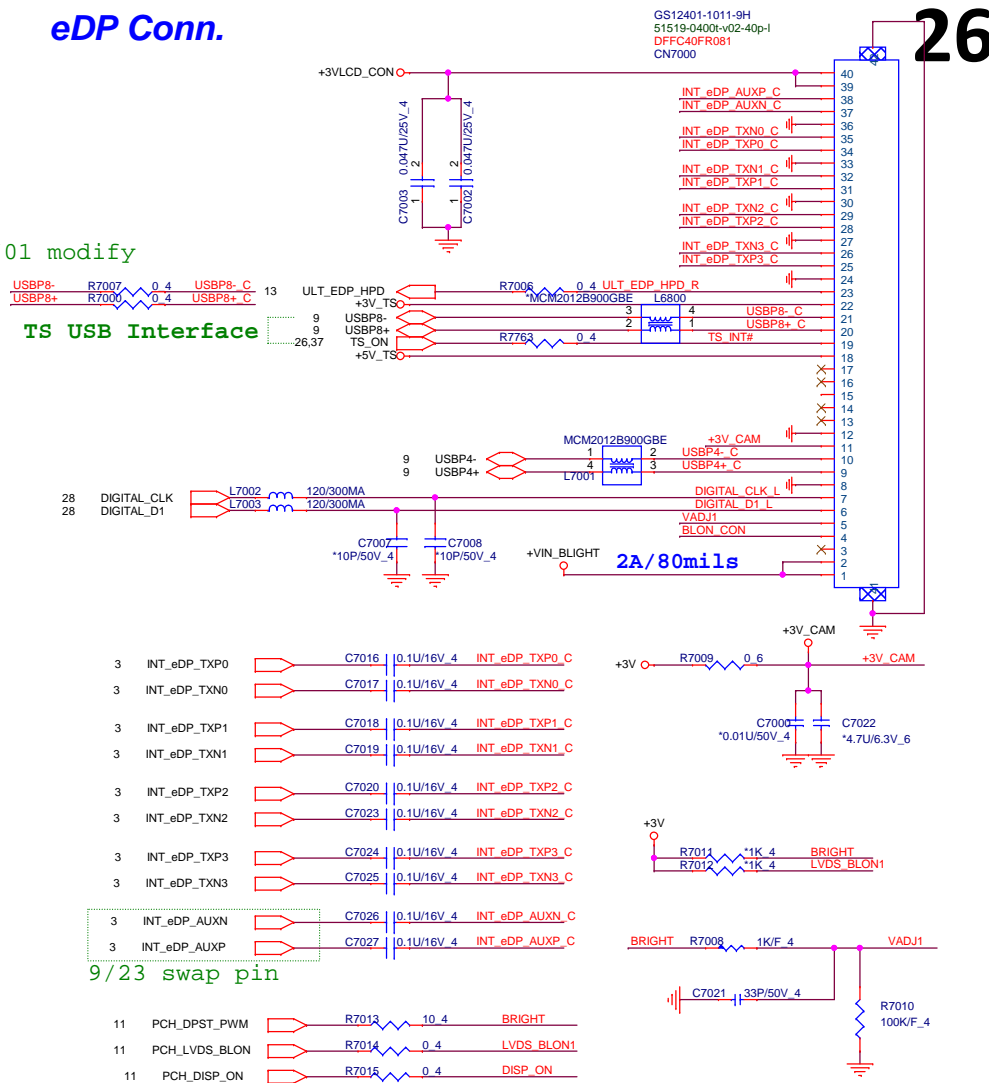
Touch screen



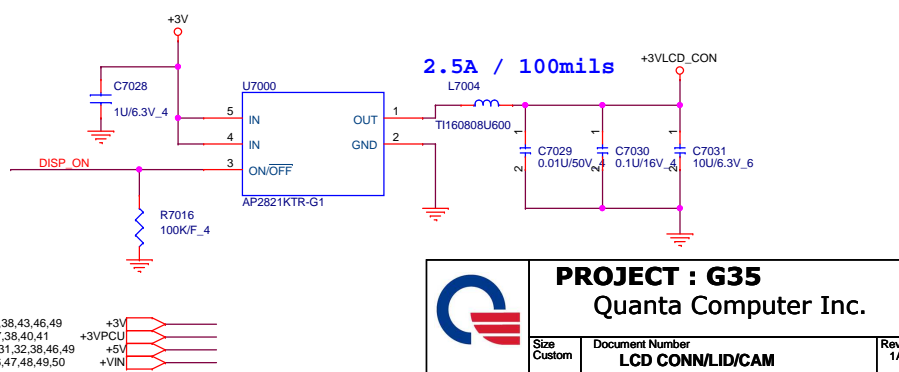
eDP Conn.

10/01 modify

TS USB Interface



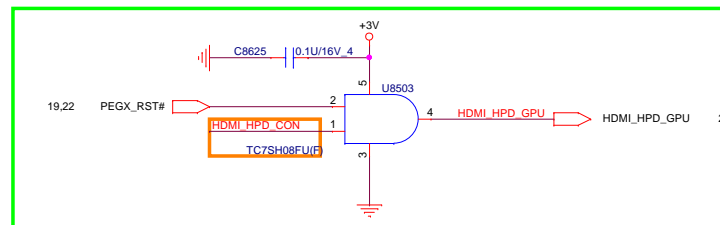
9/23 swap pin



27

| | | | |
|-----------|-------|---------|-----------|
| TX2_HDMI+ | R7716 | 120/F 4 | TX2_HDMI- |
| TX1_HDMI+ | R7717 | 120/F 4 | TX1_HDMI- |
| TX0_HDMI+ | R7719 | 120/F 4 | TX0_HDMI- |
| TXC_HDMI+ | R7722 | 120/F 4 | TXC_HDMI- |

| Pin | Signal | Function | IO Type | IO Voltage | IO Width | Signal |
|-----|-------------|----------|----------|------------|----------|-----------|
| 21 | GPU_D0 | C7723 | 0.1U/16V | 4 | | TX0 HDMI+ |
| 21 | GPU_D0# | C7724 | 0.1U/16V | 4 | | TX0 HDMI- |
| 21 | GPU_D1 | C7721 | 0.1U/16V | 4 | | TX1 HDMI+ |
| 21 | GPU_D1# | C7722 | 0.1U/16V | 4 | | TX1 HDMI- |
| 21 | GPU_D2 | C7725 | 0.1U/16V | 4 | | TX2 HDMI+ |
| 21 | GPU_D2# | C7726 | 0.1U/16V | 4 | | TX2 HDMI- |
| 21 | GPU_CLK | C7727 | 0.1U/16V | 4 | | TXC HDMI+ |
| 21 | GPU_CLK# | C7729 | 0.1U/16V | 4 | | TXC HDMI- |
| 21 | GPU_DDCCLK | | | | | |
| 21 | GPU_DDCDATA | | | | | |



Close to HDMI connector


The diagram illustrates the pin connections for the CPDA10RSV0P-HF component, specifically for the TX0 and TX1 HDMI connectors. The component is represented by a central rectangle with pins numbered 1 through 10 on both sides. The connections are as follows:

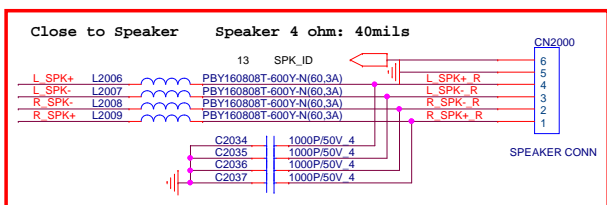
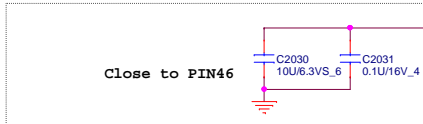
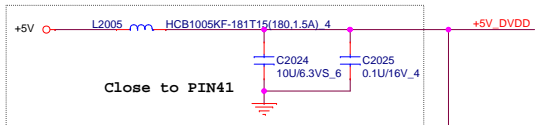
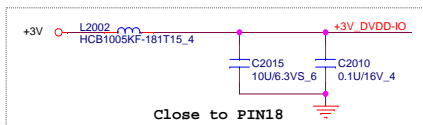
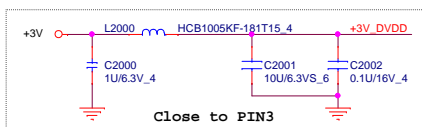
| Pin | TX0 HDMI-CN | TX1 HDMI-CN |
|-----|-------------|-------------|
| 1 | IN1 | IN1 |
| 2 | IN2 | IN2 |
| 3 | GND | GND |
| 4 | IN3 | IN3 |
| 5 | IN4 | IN4 |
| 6 | NC | NC |
| 7 | NC | NC |
| 8 | NC | NC |
| 9 | NC | NC |
| 10 | NC | NC |

The component is labeled "CPDA10RSV0P-HF" at the bottom.

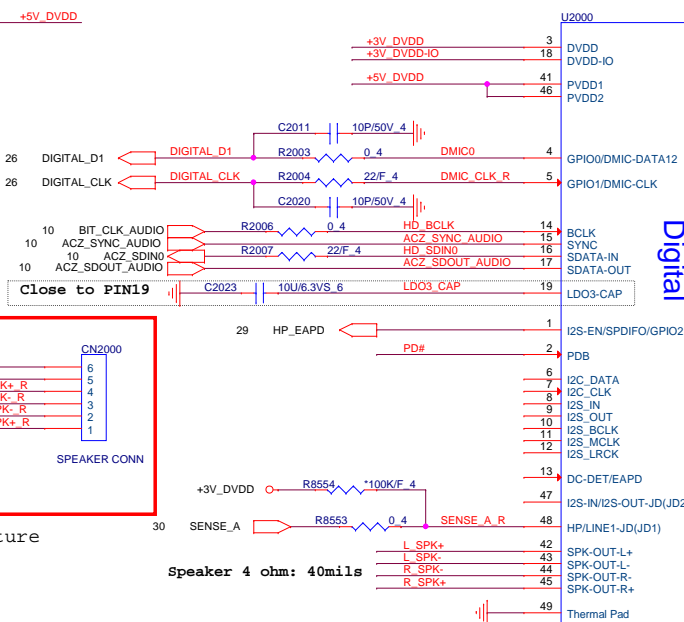
The schematic diagram illustrates the HDMI HPD (Hot Plug Detect) circuit. Key components and connections include:

- Power Supply:** +5V_AON is connected to the +5V_HDMIC line. A 40 mils trace leads to a fuse F7701 (FUSE1A6V_POLY) and a diode D7701 (BAT54AW-L).
- HPD Signal Path:** The HPD signal is connected to the HPD pin of the HDMI connector CN7701. It passes through a resistor R7745 (1M_4) and a capacitor C7740 (0.1U/16V_4) to the +5V_HDMI line.
- Signal Lines:** HDMI_SCLK and HDMI_SDATA lines are connected to the SCLK and SDATA pins of the HDMI connector.
- Resistors:** R7751 (2.2K_4) and R7752 (2.2K_4) are connected to the SCLK and SDATA lines. R7747 (20K/F_4) is connected to the HPD pin.
- Capacitors:** C7730 (*10P/50V_4) and C7731 (*10P/50V_4) are connected to the SCLK and SDATA lines. C7741 (220P/50V_4) is connected to the HPD pin.
- Diode:** D7701 (BAT54AW-L) is connected to the +5V_HDMIC line.
- Connector:** CN7701 is the HDMI connector with pins for D2+, D2-, D1+, D1-, D0+, D0-, CK+, CK-, DDC CLK, DDC DATA, GND, HP DET, and SHIELD2.

| | | | |
|---|--|-----------------|---------|
|  | PROJECT : G35 Quanta Computer Inc. | | |
| | Size Custom | Document Number | Rev 1/1 |
| | 27 -- HDMI/HDMI REDRIVER | | |
| Date: Thursday, December 24, 2015 | 1 Sheet | 27 of | 51 |



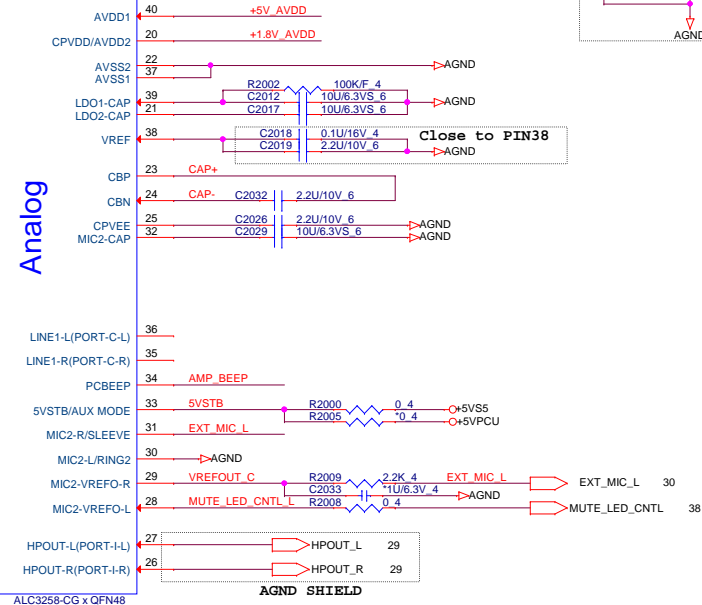
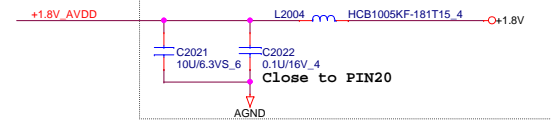
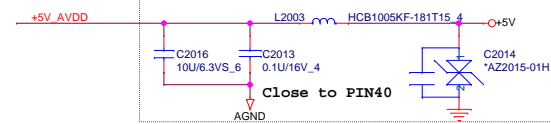
1124 Add SPK_ID for Smart amp feature



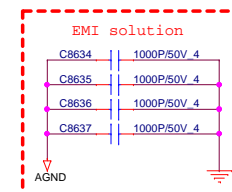
Speaker 4 ohm: 40mils

ALC3258-CG x QFN48

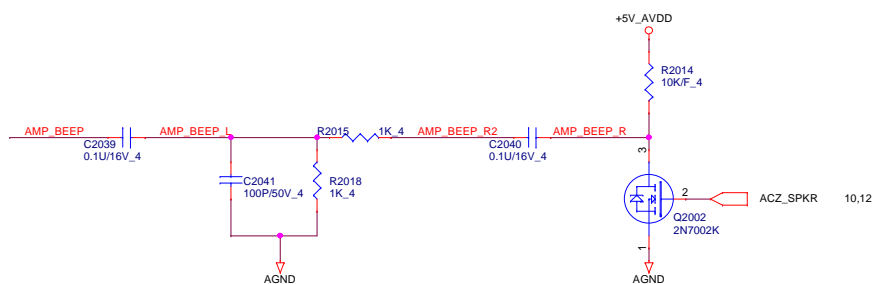
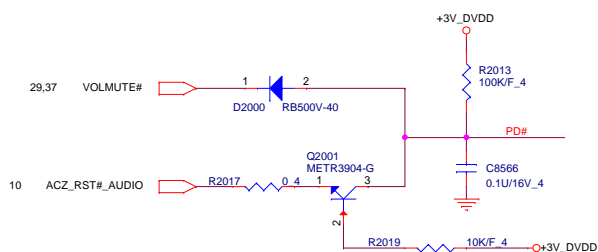
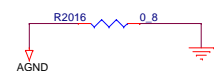
+5V_AVDD >40mils trace

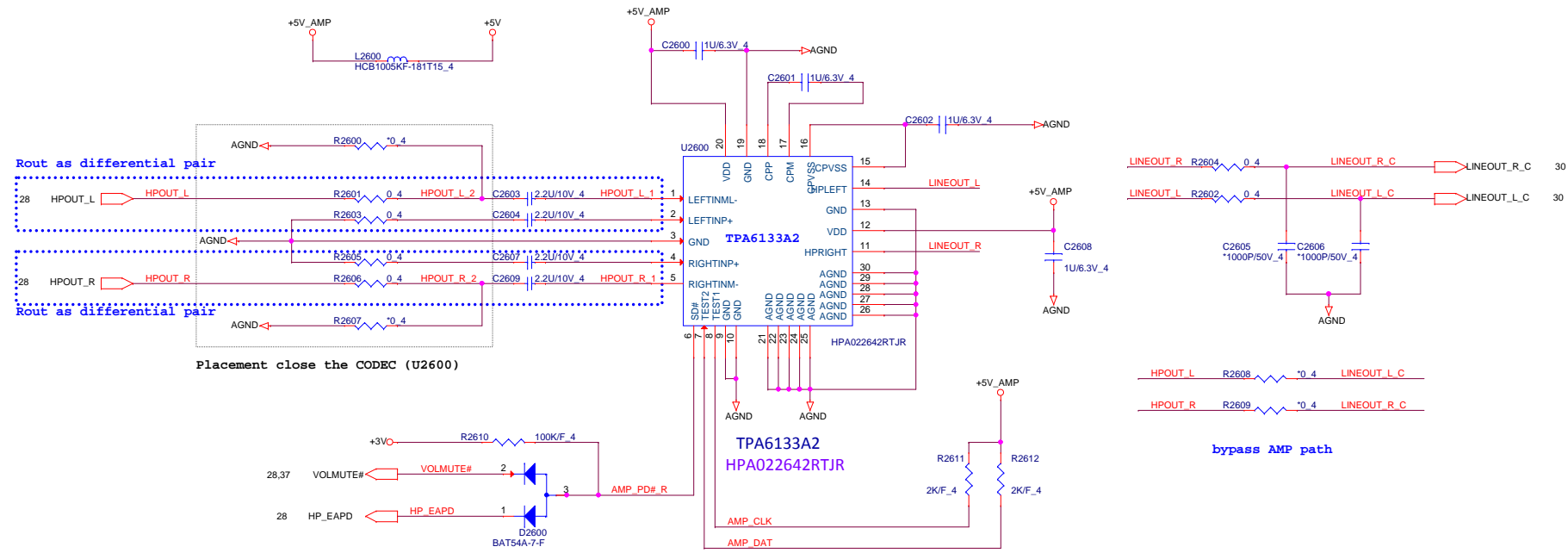


1123 Add 1000P for EMI request

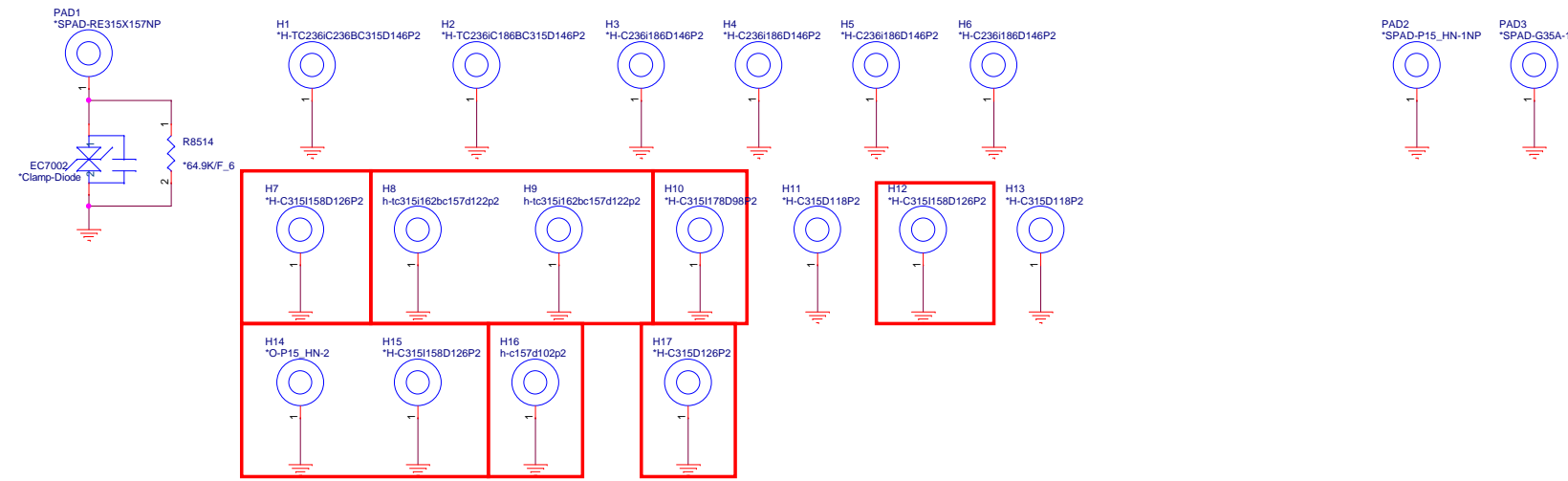


place to near or under codec

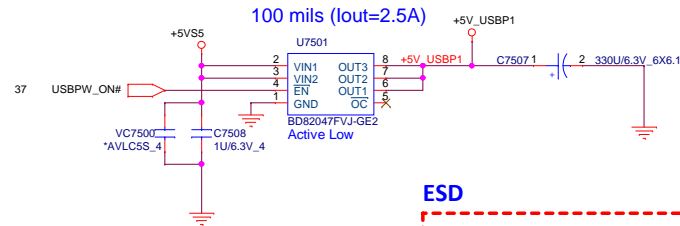




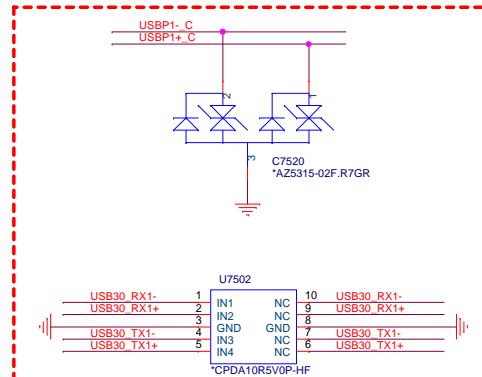
HOLE



USB 2.0/3.0 Combo



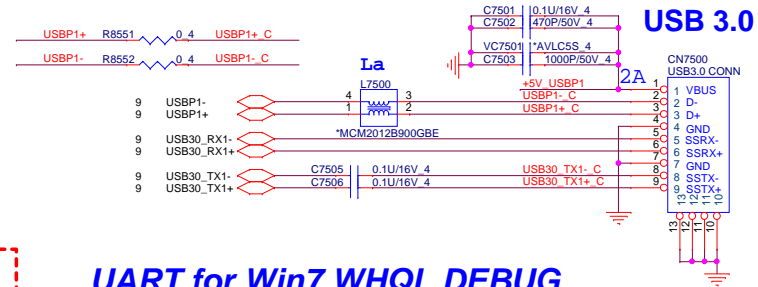
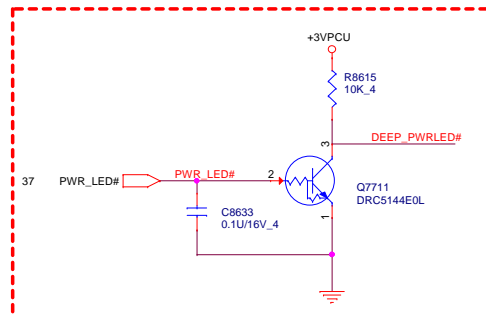
ESD



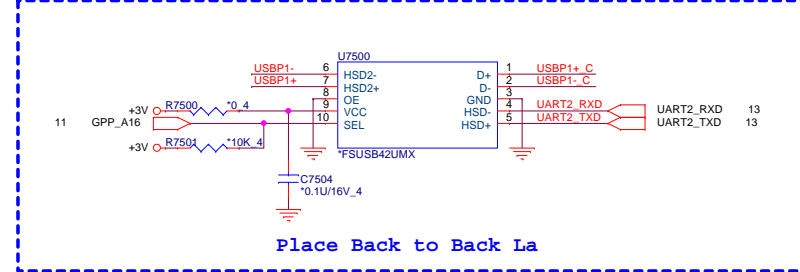
1125 Reserve ESD protection component

Daughter Board

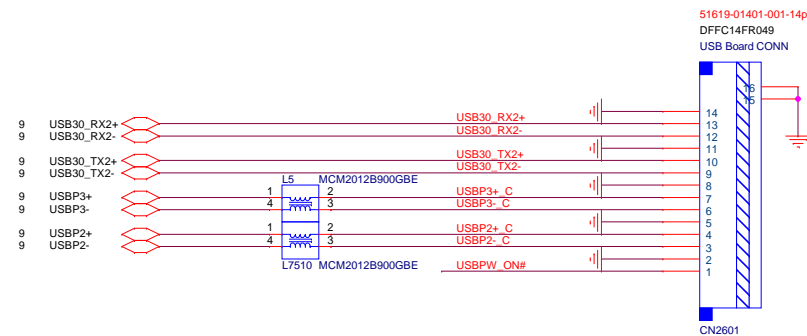
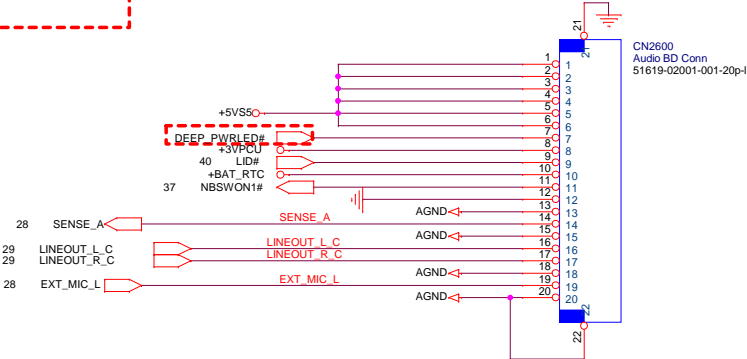
1123 Add PWR LED MOS Circuit



UART for Win7 WHQL DEBUG

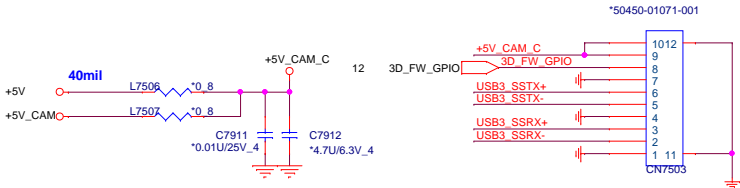


Place Back to Back La



10/08 3D Camera MIC combine in LCD CONN

3D Camera Conn.

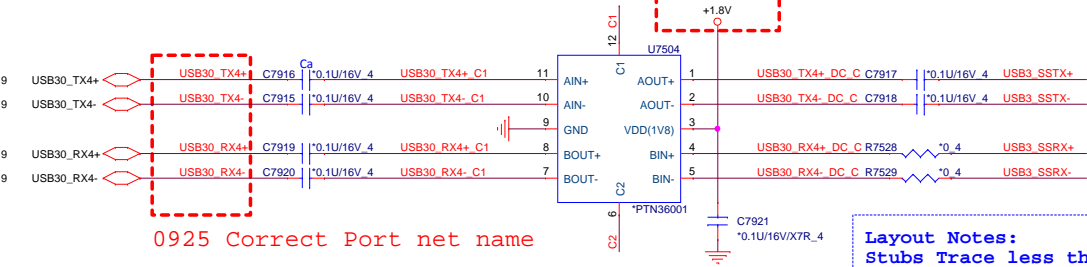


USB3.0

USB3.0 Re-driver IC

USB3.0 re-driver IC

1123 Change UB3 re driver power rail from +1.8V_DEEP_SUS to +1.8V



1123 Change UB3 re driver power rail from +1.8V_DEEP_SUS to +1.8V

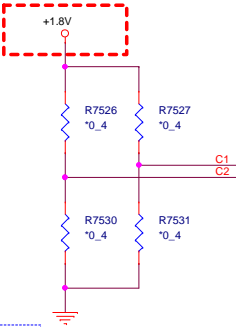


Table 4. C1 pin controls long/medium/short traces

| State | Channel type | Pin C1 state | Channel B | Channel A | |
|--------|--------------|--------------|-------------------|-------------------|-------------------|
| | | | EQ ^[1] | DE ^[2] | OS ^[3] |
| H | Long | H | 9 dB | -5.3 dB | 1.1 V |
| high-Z | Medium | high-Z | 6 dB | -3.1 dB | 1.0 V |
| L | Short | L | 3 dB | 0 dB | 0.9 V |

Table 5. C2 pin controls long/medium/short traces

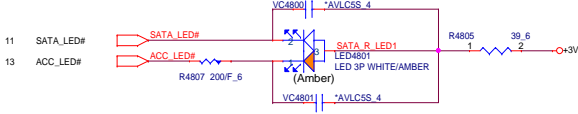
| State | Channel type | Pin C2 state | Channel A | Channel B | |
|--------|--------------|--------------|-------------------|-------------------|-------------------|
| | | | EQ ^[1] | DE ^[2] | OS ^[3] |
| H | Long | H | 9 dB | -5.3 dB | 1.1 V |
| high-Z | Medium | high-Z | 6 dB | -3.1 dB | 1.0 V |
| L | Short | L | 3 dB | 0 dB | 0.9 V |

28,40,41,46,51 +5VPCU
5,10,30,33,37,38,40,41 +3VPCU
28,47 +1.8V

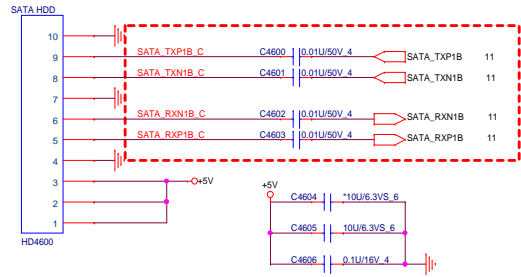


PROJECT : G35
Quanta Computer Inc.

SATA LED



HDD



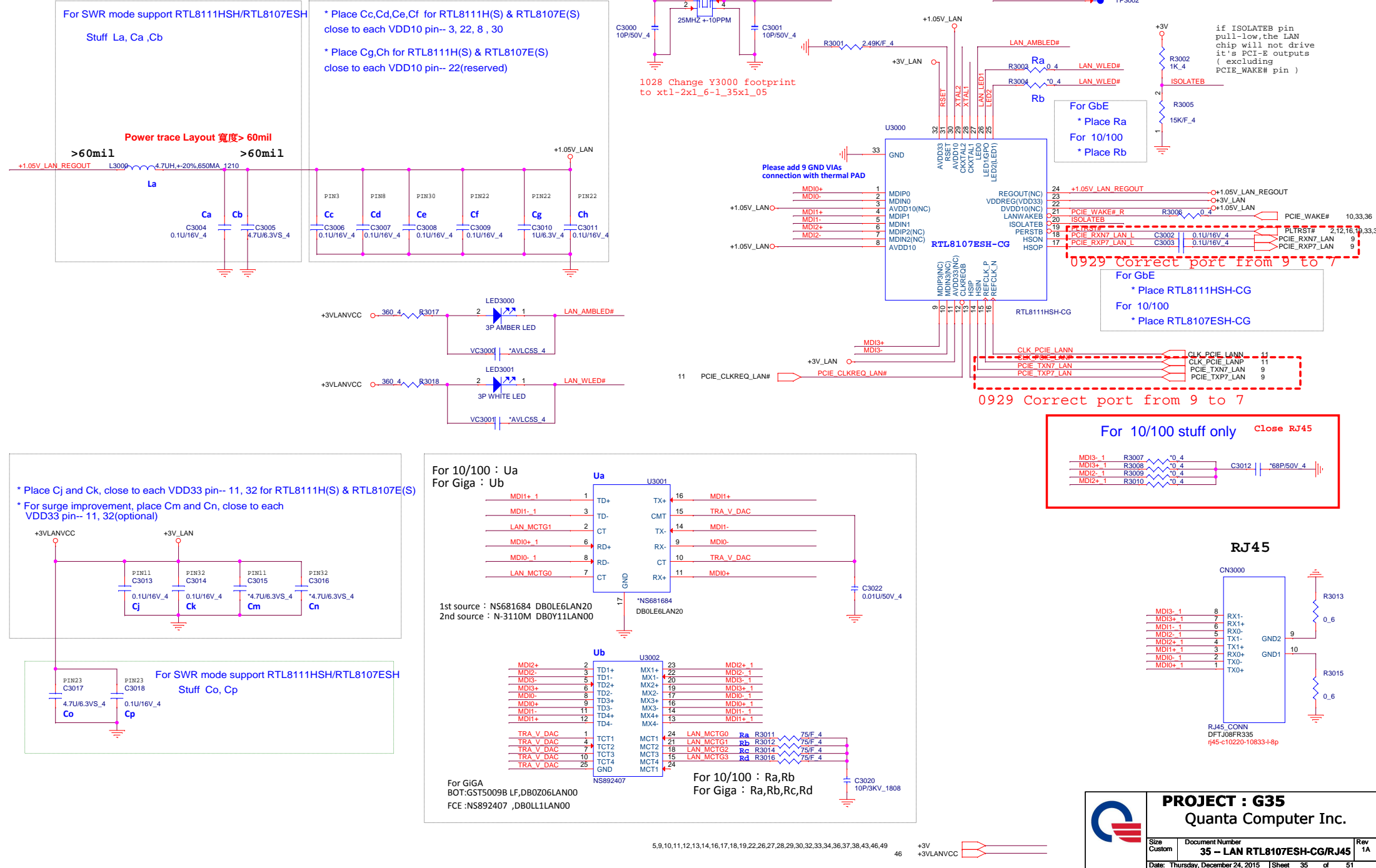
PROJECT : G35
Quanta Computer Inc.

| | | |
|--|---|-----------|
| Size C | Document Number 32 -- HDD/ODD | Rev 1A |
| Date: Thursday, December 24, 2015 Sheet 32 of 51 | | |

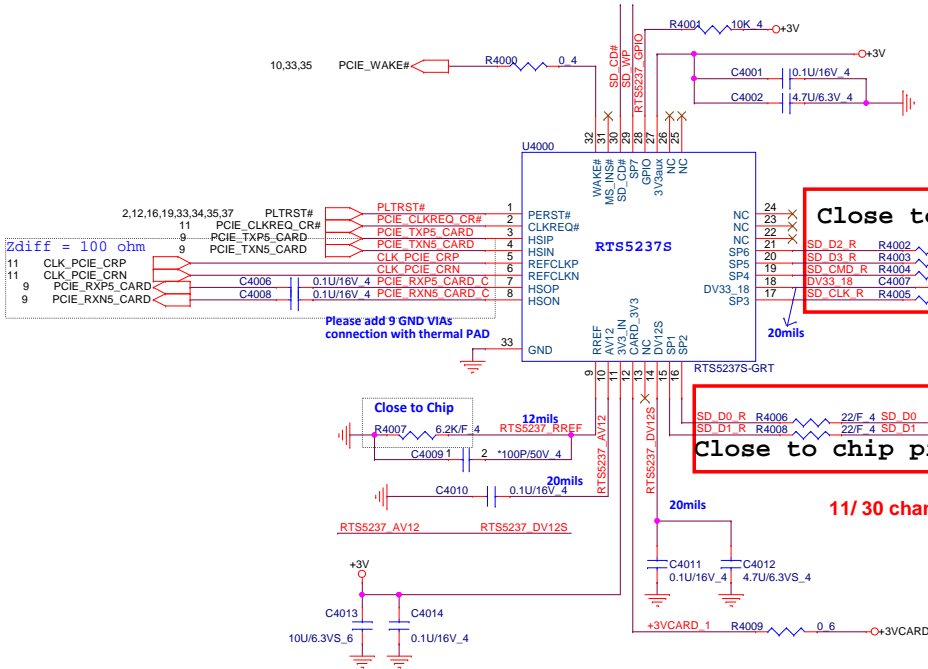


PROJECT : G35
Quanta Computer Inc.

| | | |
|-----------------------------------|--|----------------|
| Size Custom | Document Number 33 -- SSD/WLAN | Rev 1A |
| Date: Thursday, December 24, 2015 | | Sheet 33 of 51 |

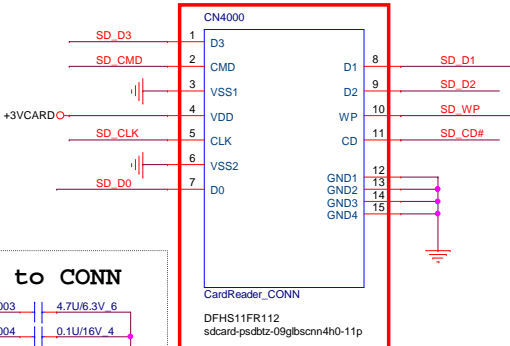


5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,37,38,43,46,49 +3V



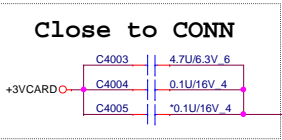
| | | |
|-----|--------|--------|
| SP1 | SD_D1 | |
| SP2 | SD_D0 | MS_D1 |
| SP3 | SD_CLK | MS_D0 |
| SP4 | SD_CMD | MS_D2 |
| SP5 | SD_D3 | MS_D3 |
| SP6 | SD_D2 | MS_CLK |
| SP7 | SD_WP | MS_BS |

Share Pin
SD / MMC



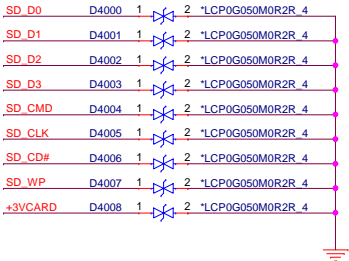
Close to chip pin

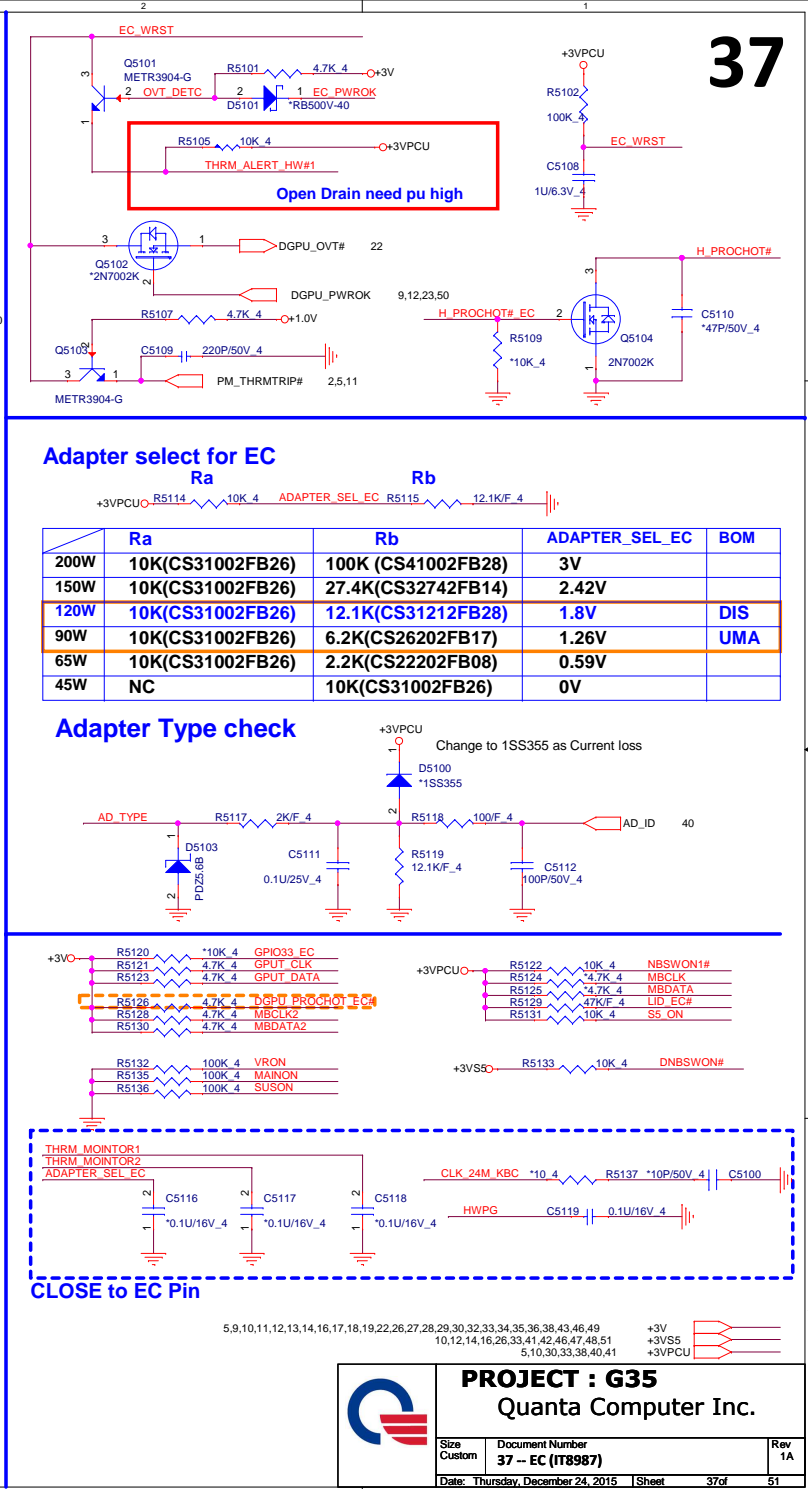
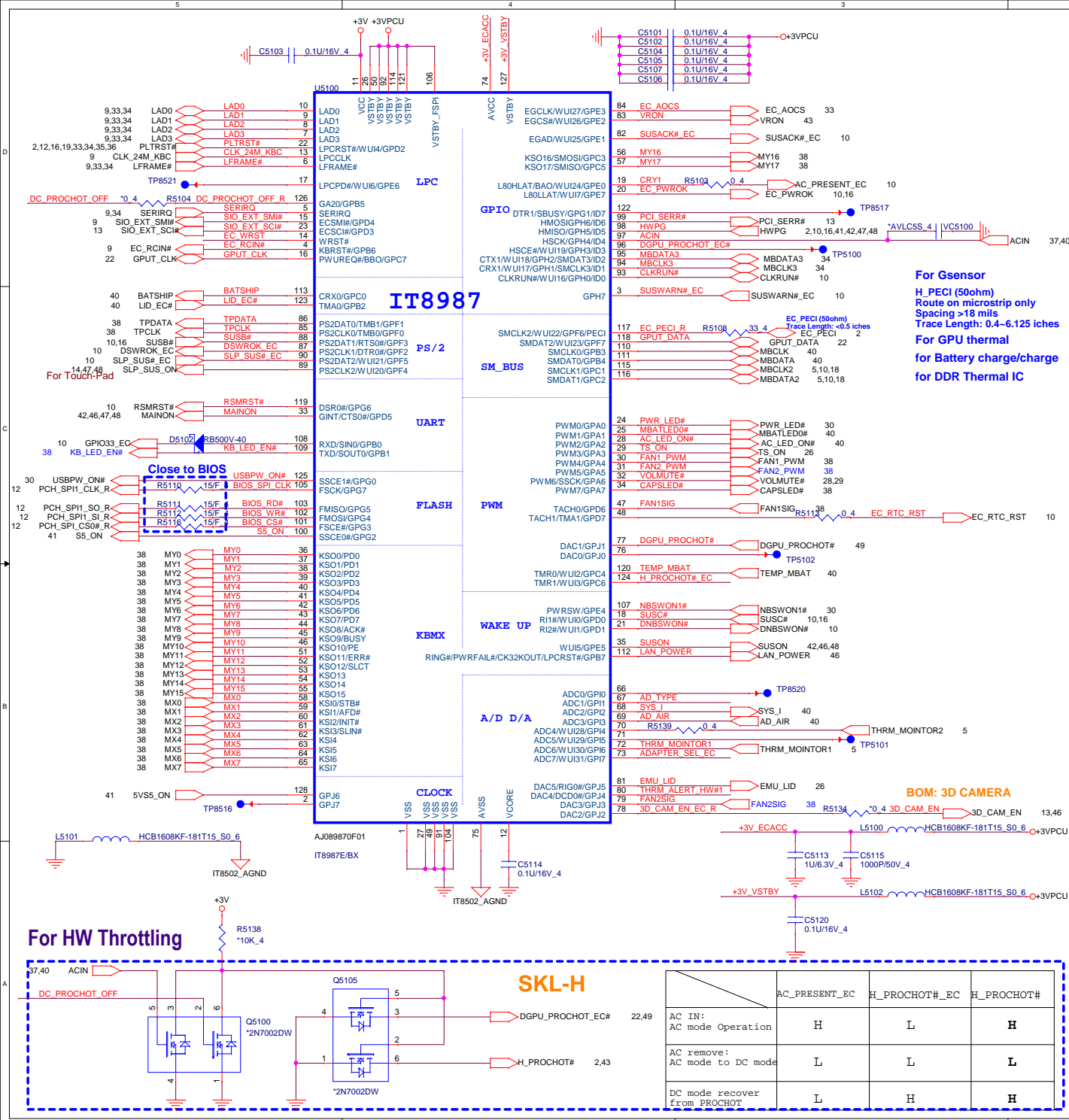
| | | |
|--------|--------|------------|
| SD_D0 | EC4000 | 5.6P/50V_4 |
| SD_D1 | EC4001 | 5.6P/50V_4 |
| SD_D2 | EC4002 | 5.6P/50V_4 |
| SD_D3 | EC4003 | 5.6P/50V_4 |
| SD_CMD | EC4004 | 5.6P/50V_4 |
| SD_CLK | EC4005 | 5.6P/50V_4 |

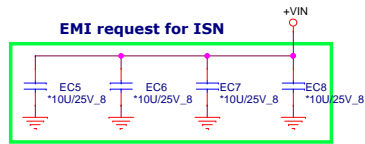
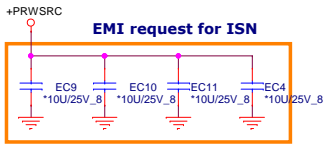


Close to chip pin

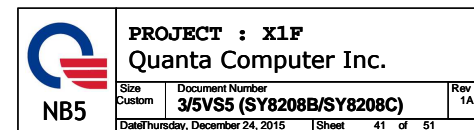
11/ 30 change to 22 ohm & stuff 5.6p for EMI request

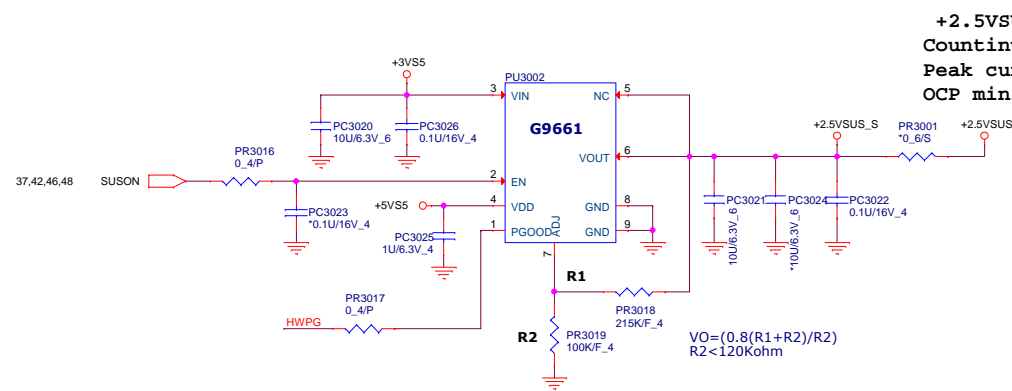
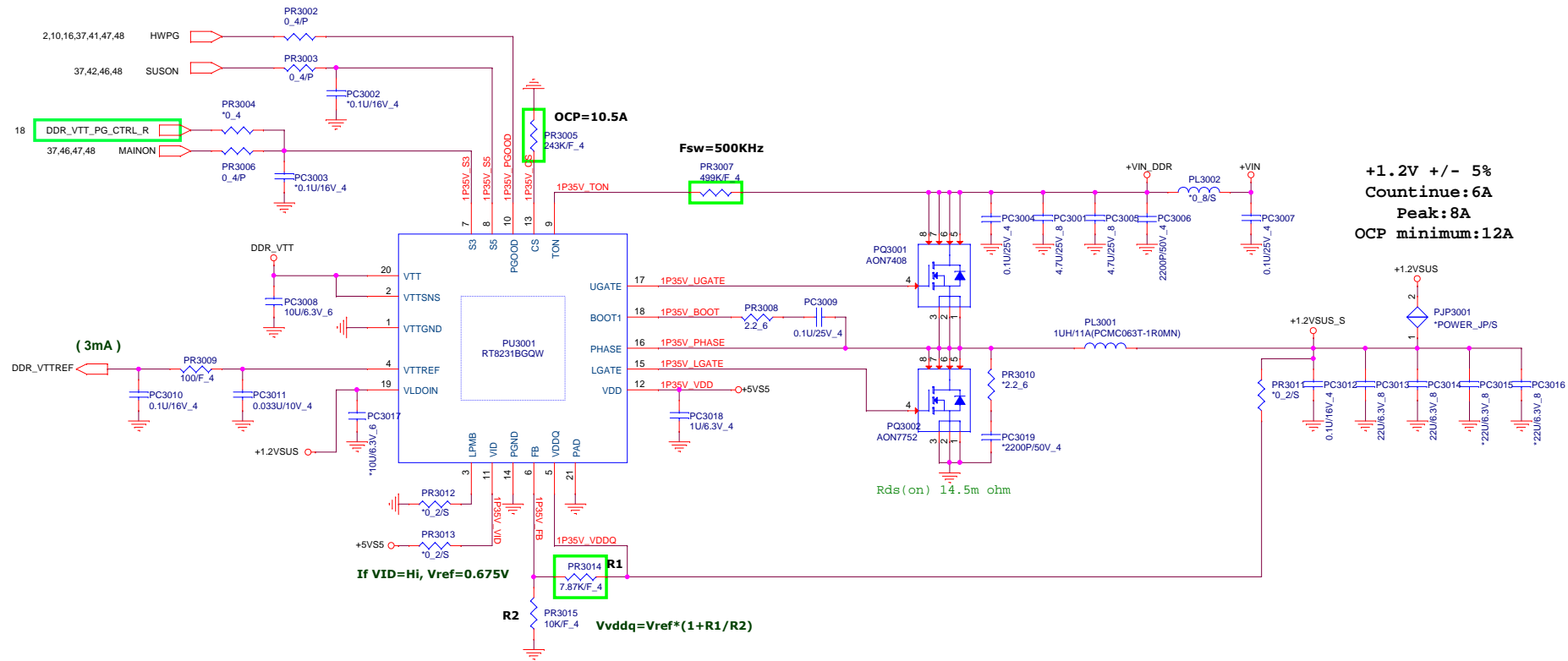




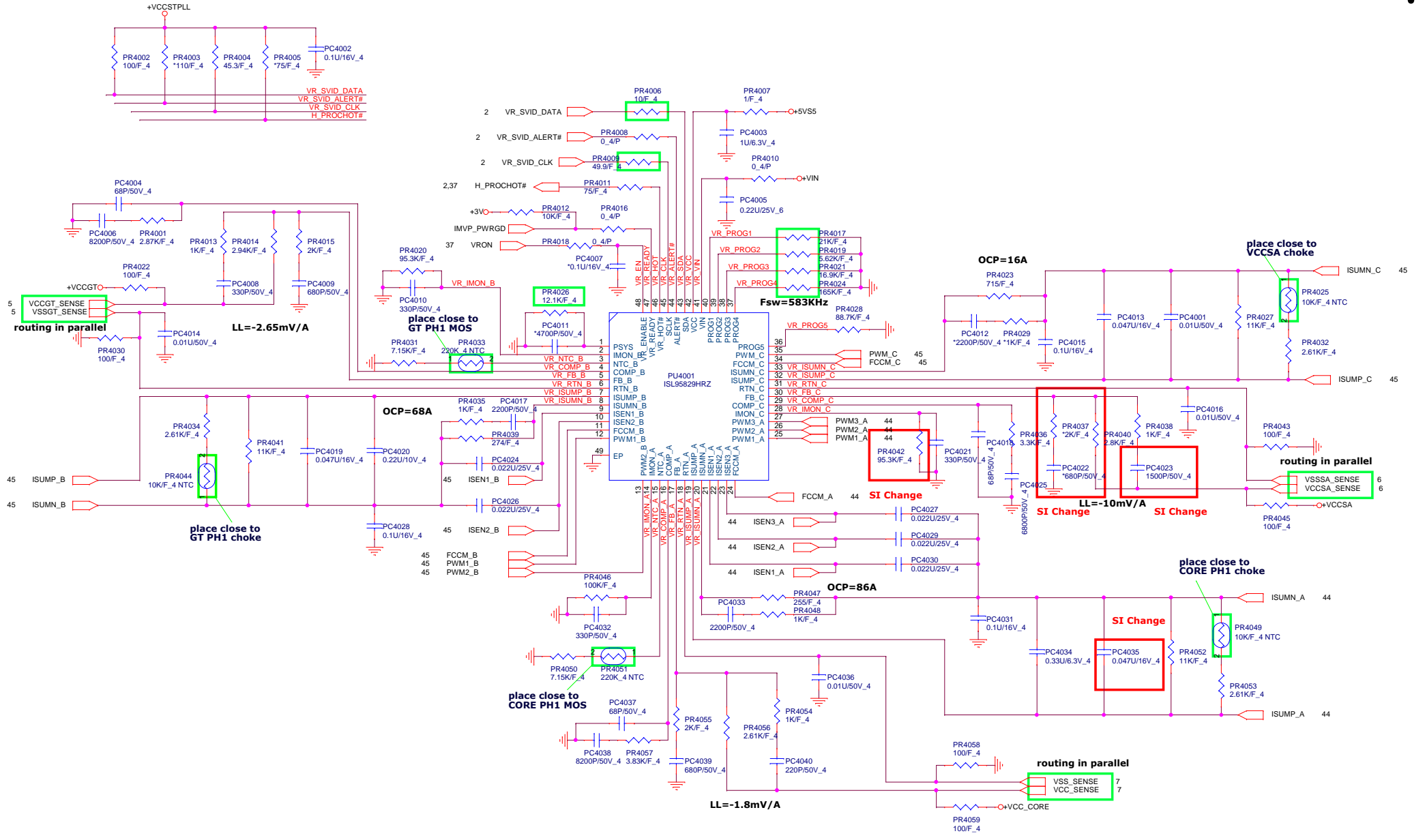


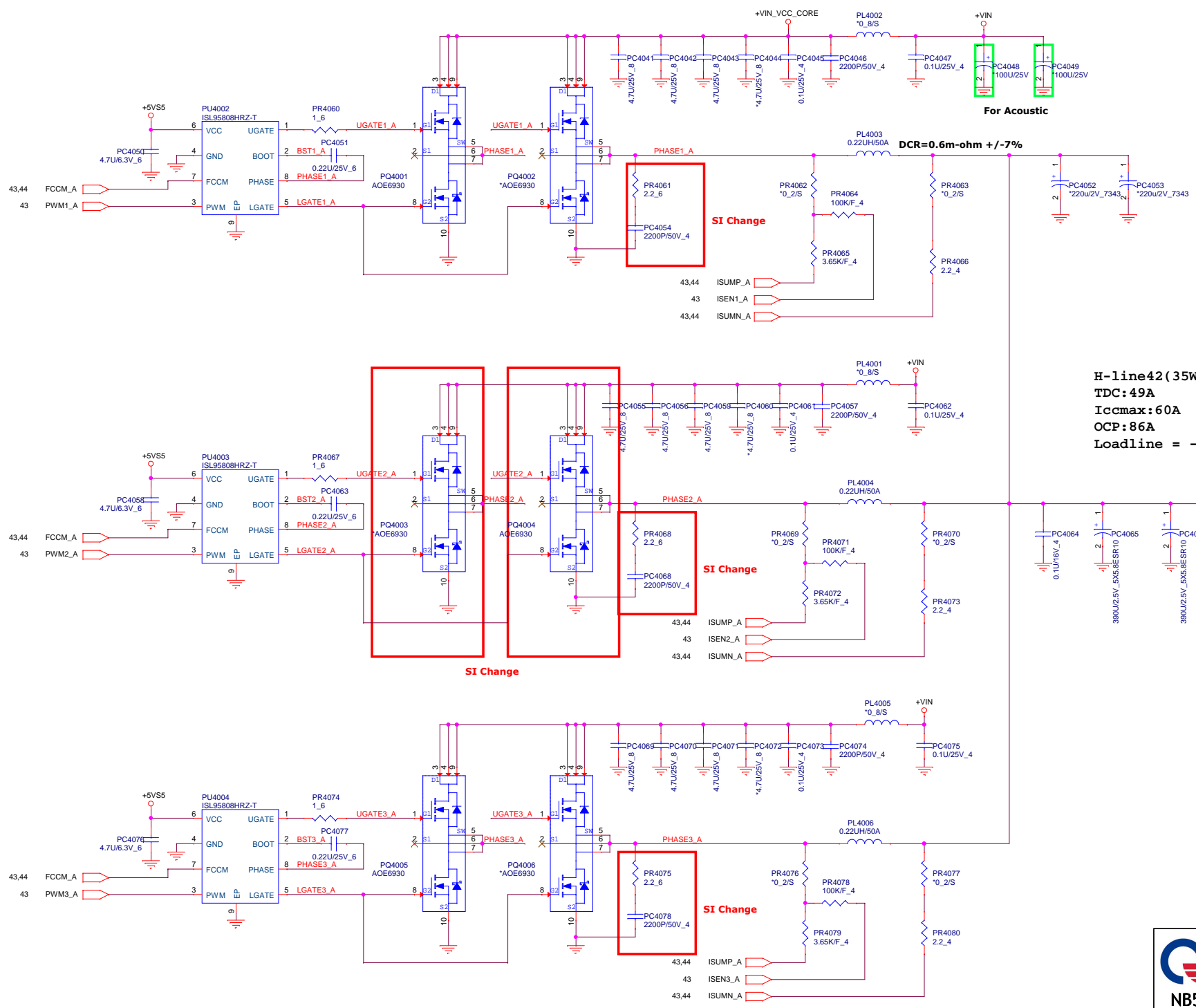






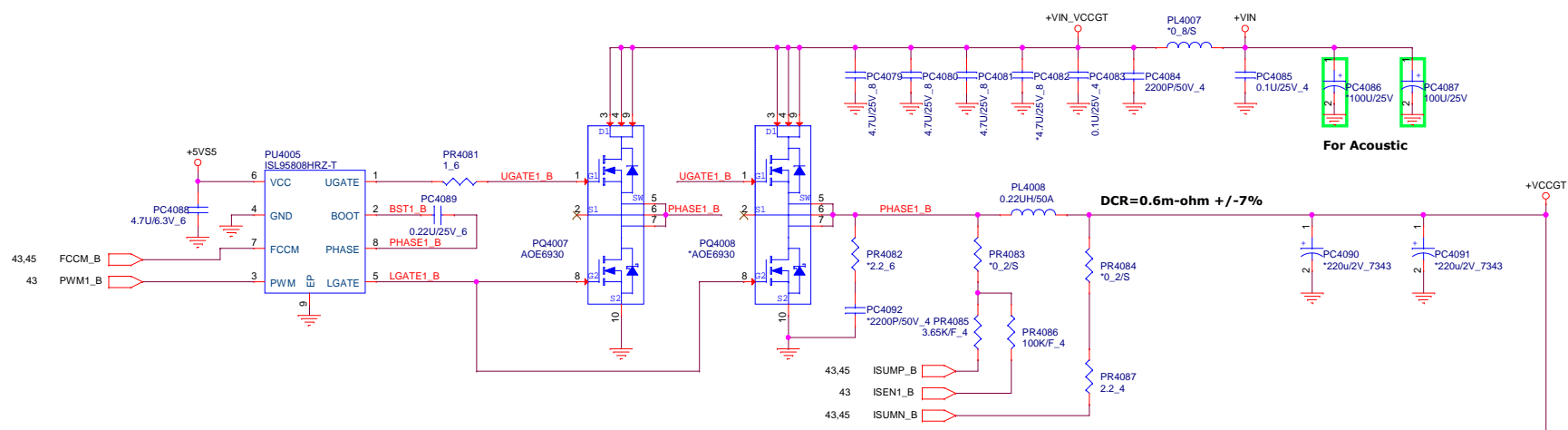
| | |
|----------|---|
| +VIN | 26,38,39,40,41,43,44,45,47,48,49,50 |
| +5VS5 | 10,26,28,30,41,43,44,45,46,47,48,49,50,51 |
| +1.2VSUS | 2,6,10,17,18,48,51 |
| DDR_VTT | 17,18 |
| +2.5VSUS | 17,18 |





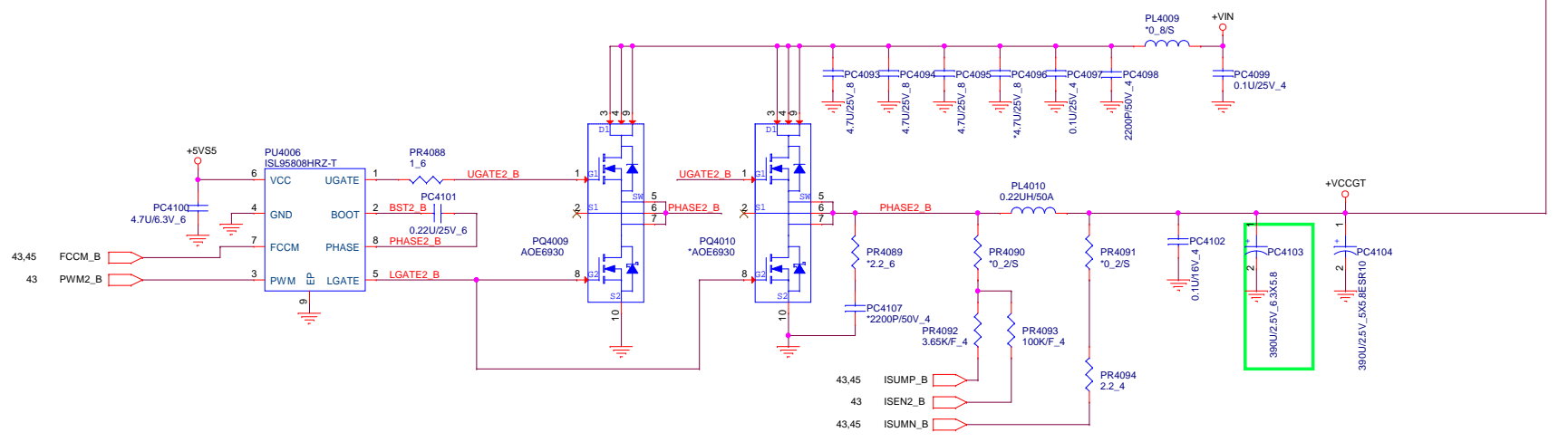
H-line42(35W)
TDC:49A
Iccmax:60A
OCP:86A
Loadline = -1.8 mV/A

H-line42(45W)
TDC:56A
Iccmax:68A
OCP:86A
Loadline = -1.8 mV/A

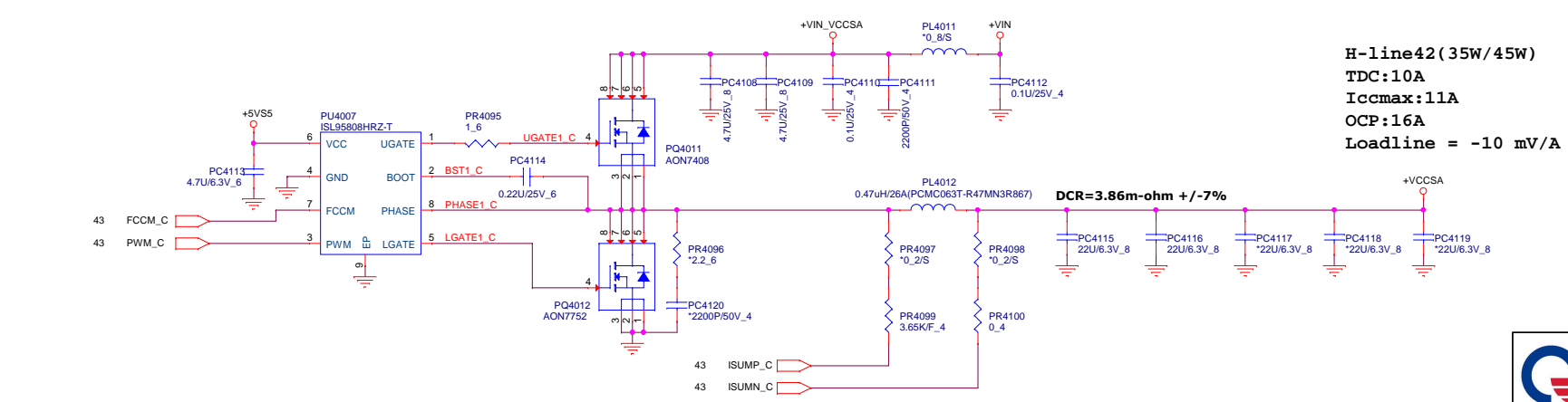


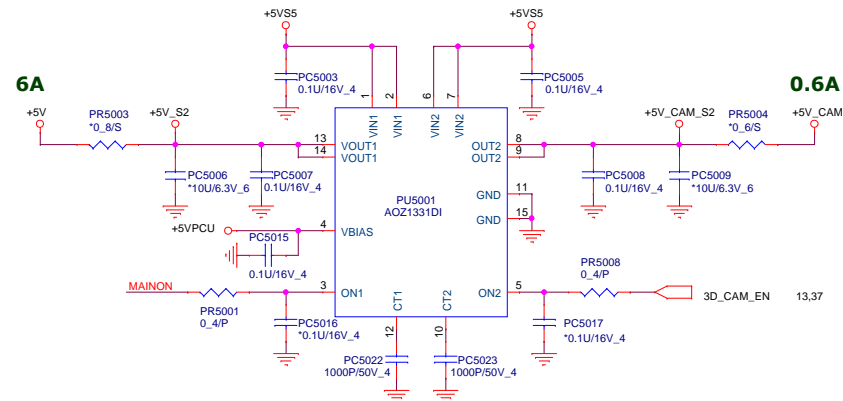
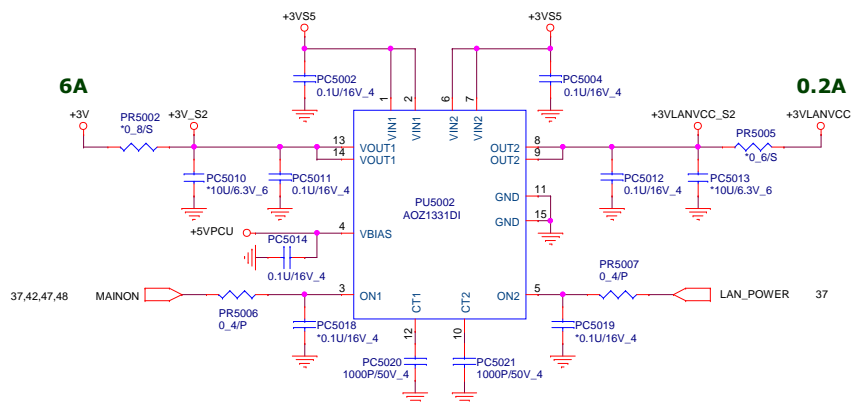
H-line42 (35W)
TDC:41A
Iccmax:55A
OCP:68A
Loadline = -2.65 mV/A

H-line42 (45W)
TDC:39A
Iccmax:55A
OCP:68A
Loadline = -2.65 mV/A

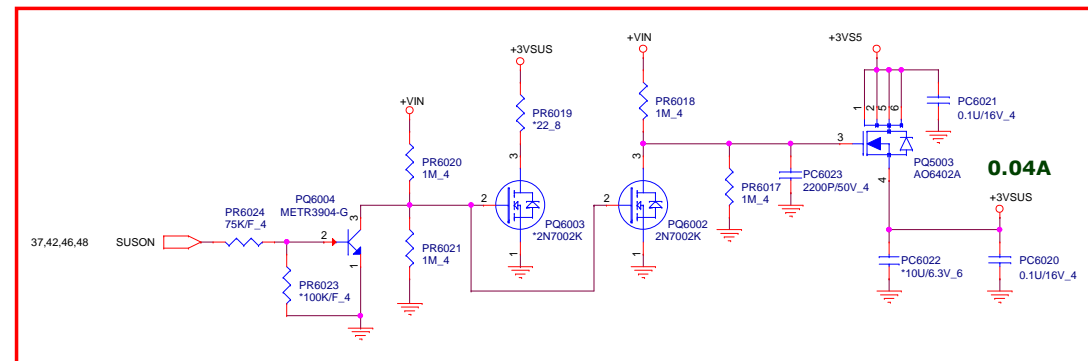


H-line42 (35W/45W)
TDC:10A
Iccmax:11A
OCP:16A
Loadline = -10 mV/A




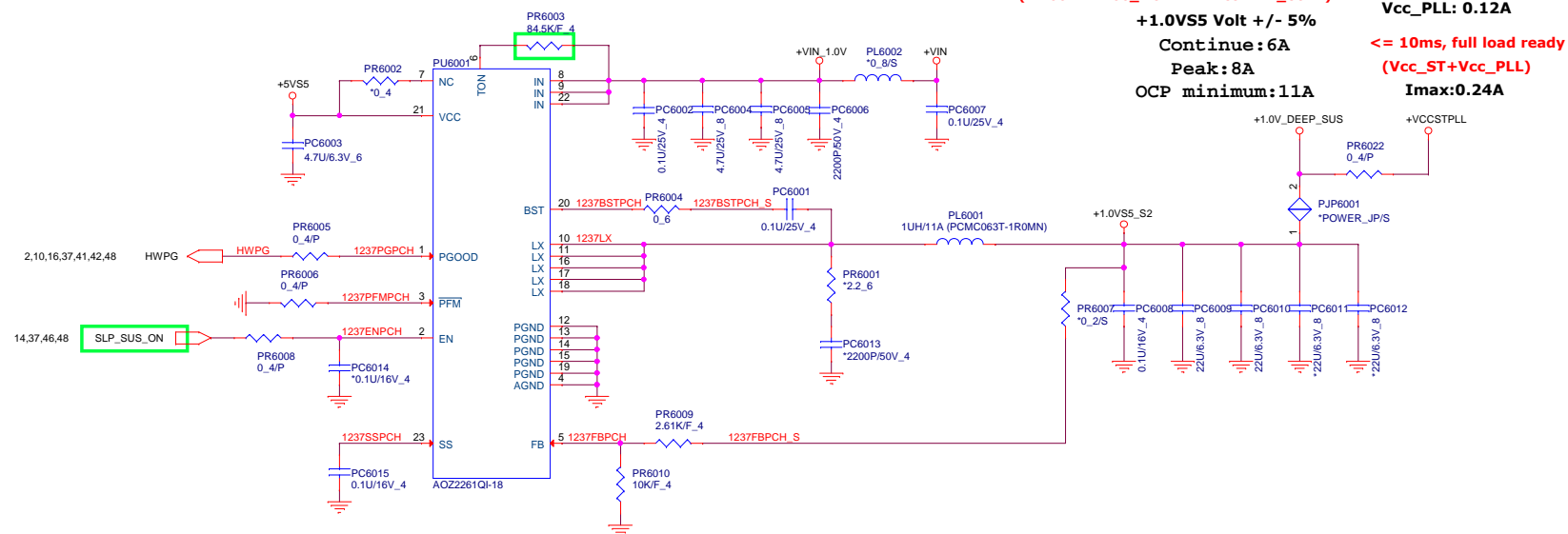


SI Change

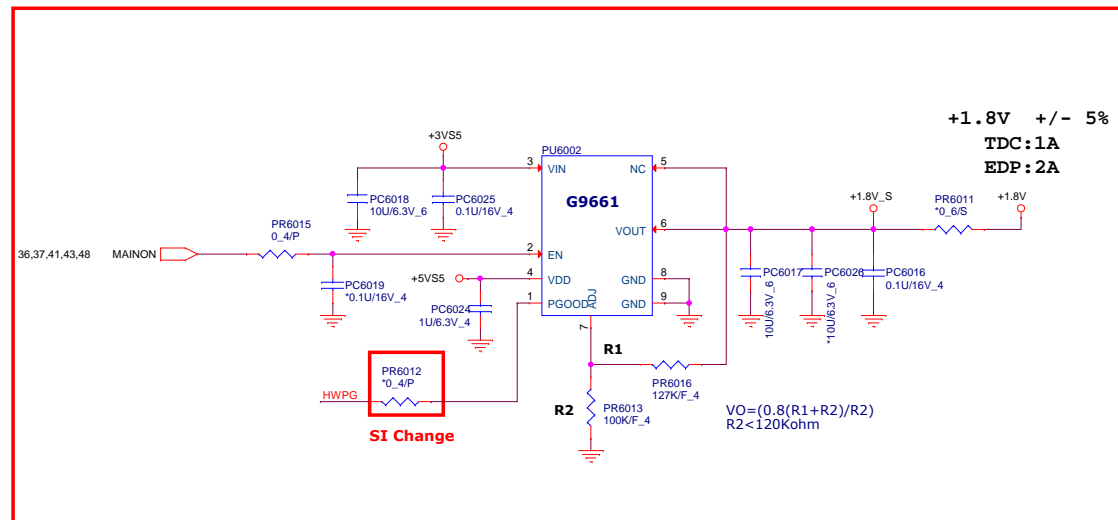


| | |
|--------------|---|
| +3V | 5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,49 |
| +5V | 26,27,28,29,31,32,38,49 |
| +3VS5 | 10,12,14,16,26,33,37,41,42,47,48,51 |
| +5VS5 | 10,26,28,30,41,42,43,44,45,47,48,49,50,51 |
| +3VSUS | 38 |
| +3VLANVCC | 35 |
| +5V_CAM | 31 |
| +3V_DEEP_SUS | 9,10,12,13,14,16,18 |

| | | |
|---|-----------------------------------|-----------------|
|  | PROJECT : X1F | |
| | Quanta Computer Inc. | |
| | Size Custom | Document Number |
| | Load switch IC (AOZ1331D) | |
| NB5 | Date: Thursday, December 24, 2015 | Sheet 46 of 51 |
| | Rev 1A | |



SI Change



| | |
|----------------|---|
| +VIN | 26,38,39,40,41,42,43,44,45,46,49,50 |
| +3VS5 | 10,12,14,16,26,33,37,41,42,46,48,51 |
| +5VS5 | 10,26,28,30,41,42,43,44,45,46,48,49,50,51 |
| +1.0V_DEEP_SUS | 10,11,14,16,48 |
| +1.8V_DEEP_SUS | 31 |
| +1.8V | 28 |
| +VCCSTPLL | 2,6,43 |

Volume Segment

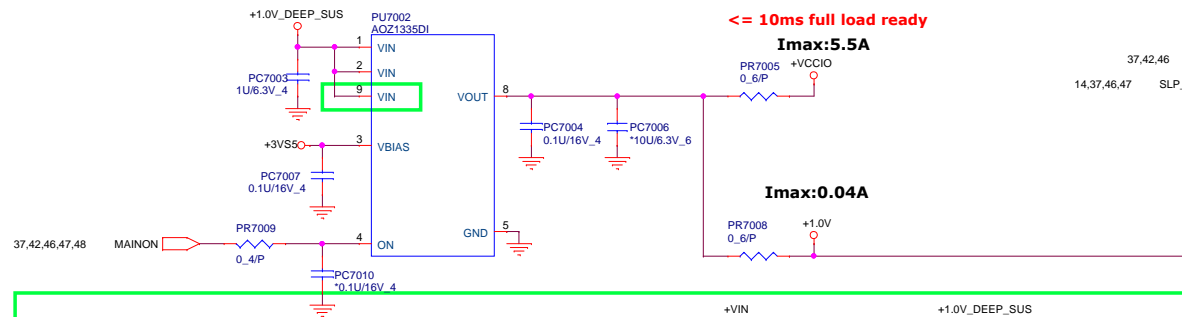
Vcc_STG: 0.04A

Vcc_IO: 5.5A

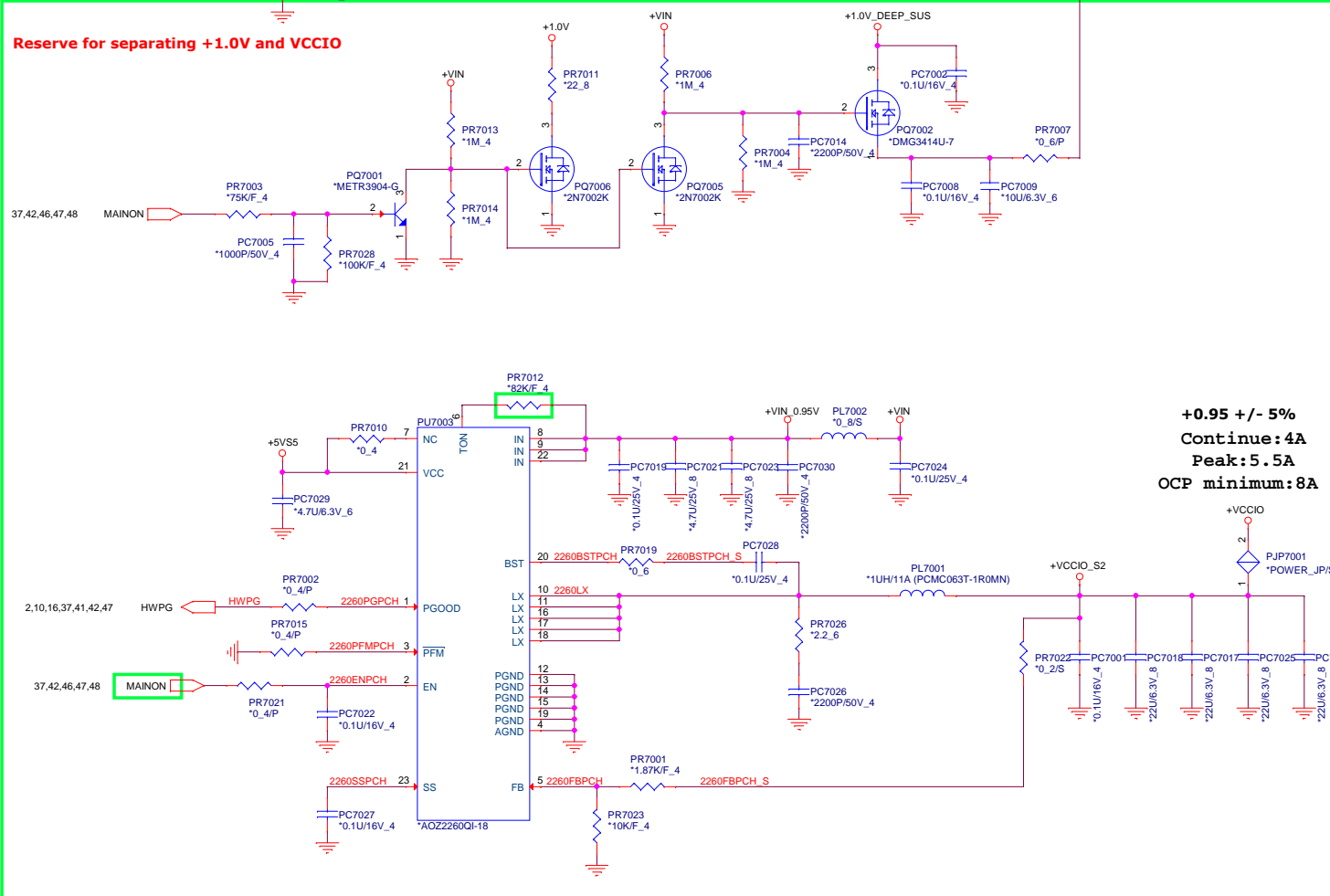
<= 10ms full load ready

Imax:5.5A

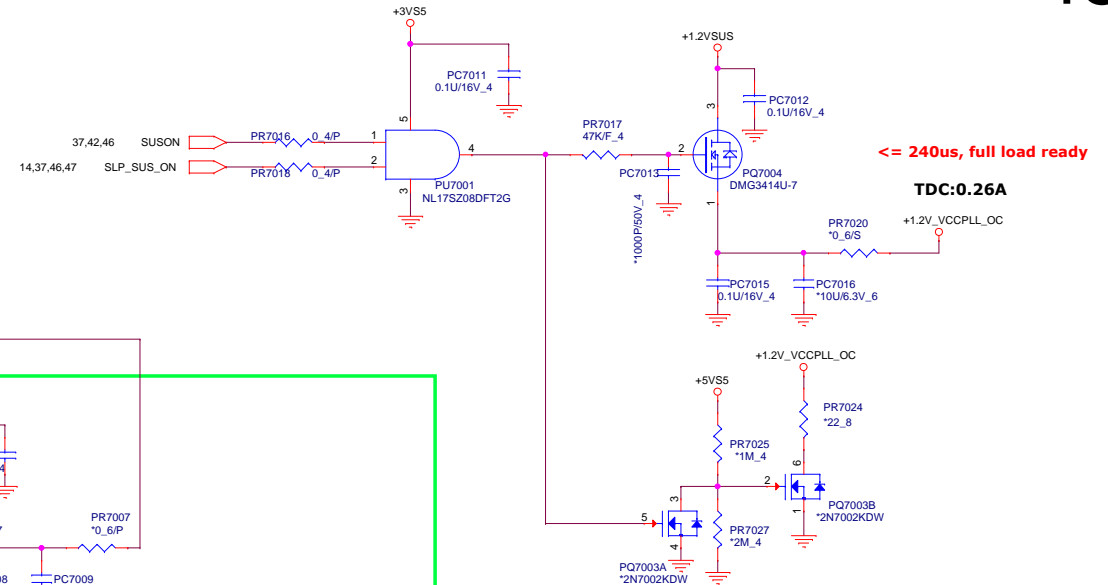
Imax:0.04A



Reserve for separating +1.0V and VCCIO



+0.95 +/- 5%
Continue:4A
Peak:5.5A
OCP minimum:8A



<= 240us, full load ready

TDC:0.26A

| | |
|-----------------|---|
| +1.0V | 2,5,6,10,16,37 |
| +3VS5 | 10,12,14,16,26,33,37,41,42,46,47,51 |
| +5VS5 | 10,26,28,30,41,42,43,44,45,46,47,49,50,51 |
| +VCCIO | 3,6,16 |
| +1.0V_DEEP_SUS | 10,11,14,16,47 |
| +1.2V_VCCPLL_OC | 6 |
| +1.2VSUS | 2,6,10,17,18,42,51 |

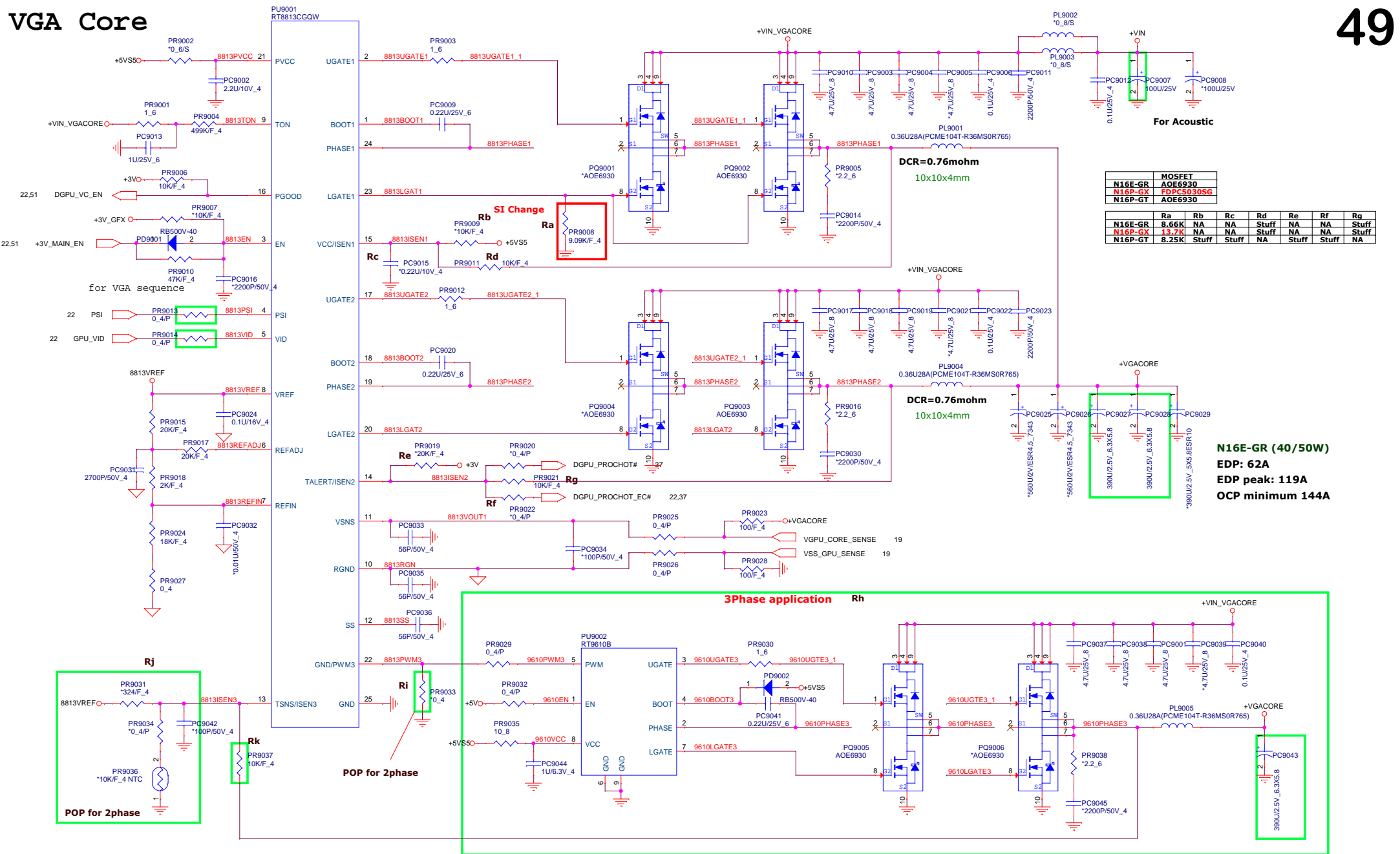


PROJECT : X1F
Quanta Computer Inc.

| Size | Document Number | Rev |
|-----------------------------------|------------------------|-----|
| Custom | +1.0V/+VCCSTPLL/+VCCIO | 1A |
| Date: Thursday, December 24, 2015 | Sheet 48 of 51 | |

VGA Core

49



| | Rh | Ri | Rj | Rk |
|---------|-------|-------|-------|-------|
| N16E-GR | Stuff | NA | NA | Stuff |
| N16P-GX | Stuff | NA | NA | Stuff |
| N16P-GT | NA | Stuff | Stuff | NA |

| | |
|----------|--|
| +3V | 5, 9, 10, 11, 12, 13, 14, 16, 17, 18, 19, 22, 26, 27, 28, 29, 30, 32, 33, 34, 35, 36, 37, 38, 43, 46 |
| +VIN | 26, 38, 39, 40, 41, 42, 43, 44, 45, 47, 48, 50 |
| +5VS5 | 10, 26, 28, 30, 41, 42, 43, 44, 45, 46, 47, 48, 50, 51 |
| +3V_GFX | 19, 20, 22, 23, 51 |
| +VGACORE | 23 |

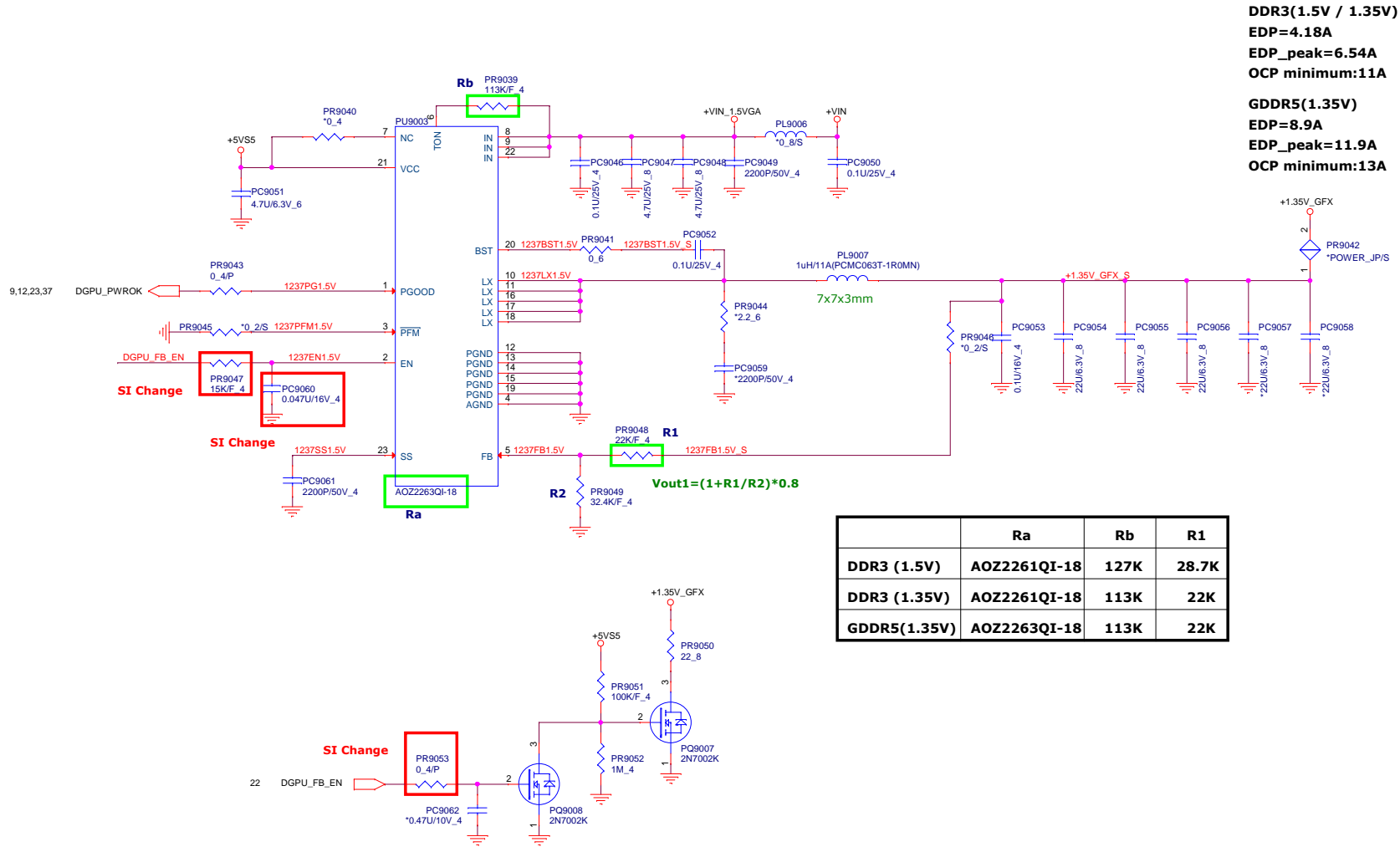
PROJECT : X1Q
Quanta Computer Inc.

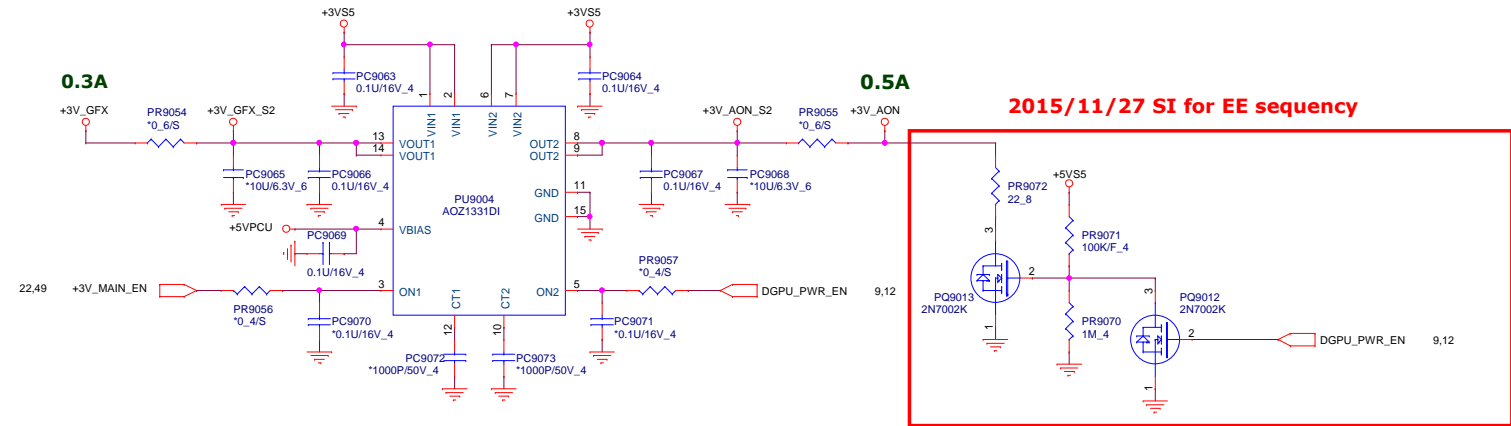
Size Custom

Document Number
+VGACORE (RT8813C)

Date: Thursday, December 24, 2015 | Sheet 49 of 51

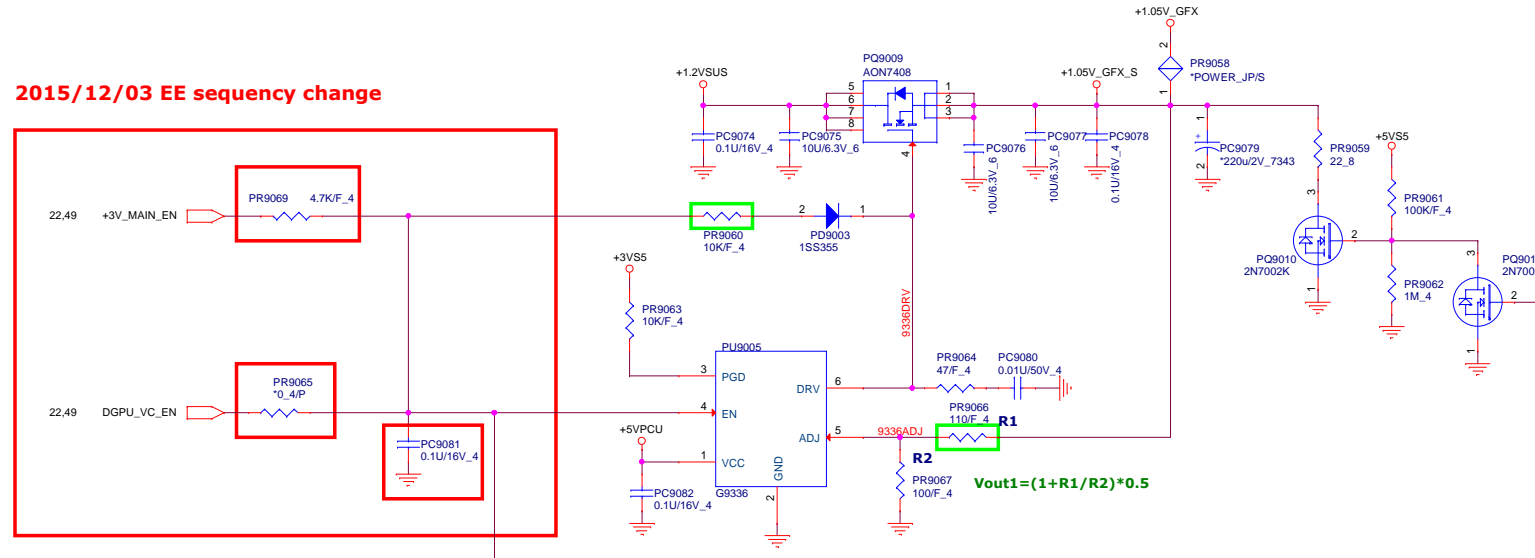
Rev 1A





+1.05V_GFX Volt +/- 5%
EDP=2.38A
EDP_peak = 2.45A

2015/12/03 EE sequence change



| | |
|------------|---|
| +VIN | 26,38,39,40,41,42,43,44,45,47,48,49,50 |
| +3VSS | 10,12,14,16,26,33,37,41,42,46,47,48 |
| +5VSS | 10,26,28,30,41,42,43,44,45,46,47,48,49,50 |
| +3V_GFX | 19,20,22,23,49 |
| +3V_AON | 19,22,23 |
| +1.2VSUS | 2,6,10,17,18,42,48 |
| +1.05V_GFX | 19,20,21,23 |